INSTRUCTION MANUAL

8015B

ELECTRONIC COUNTER

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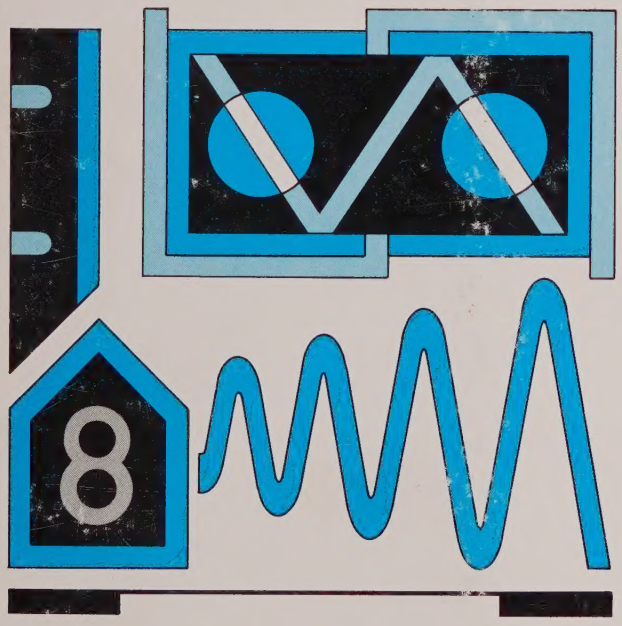

DANA®

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INSTRUCTION MANUAL

MODEL 8015B

ELECTRONIC COUNTER

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SPECIFICATIONS

FREQUENCY MEASUREMENTS to 150 MHz	
Frequency Range:	
dc coupled:	0 to 150 MHz
ac coupled:	10 Hz to 150 MHz
Accuracy:	±1 count ±reference error
Input:	Channel A
Input Characteristics:	
Sensitivity, sinewave:	50 mV rms to 100 MHz; 100 mV rms to 150 MHz
Sensitivity, pulse:	150 mV peak; 4 nsec minimum width
Impedance:	1 megohm shunted by 25 pF
Maximum input: (without damage)	250V rms or 300V peak on all ranges except 150V rms or 200V peak to 1 MHz on 1V range
Voltage ranges:	1, 10, 100 selectable
Trigger level:	Continuously adjustable to ±300% of input voltage range
Trigger slope:	+ or −, selectable
Preset condition:	0 trigger level
Measurement Time:	1 μsec to 100 seconds, selectable in decade steps
Display:	8 digits (optional 9 digits), KHz or MHz
Self Check:	10 MHz

FREQUENCY MEASUREMENTS to 550 MHz (Model 8035B)	
Frequency Range:	
ac coupled:	1 MHz to 550 MHz
Accuracy:	±1 count ±reference error
Input:	Channel C
Input Characteristics:	
Sensitivity, sinewave:	50 mV rms (1 mV with optional 030 prescaler)
Impedance:	50 ohms nominal
Maximum Input: (operating)	1V rms
Maximum Input: (without damage)	5V rms
Automatic Gain Control:	26 dB without adjustment (60 dB with option 030)

TIME INTERVAL MEASUREMENTS	
Range:	10 nsec to 10^8 sec (10^9 sec with option 004)
Resolution:	10 nsec
Accuracy:	±1 count ±reference error ±trigger error*
Input:	
separate mode:	Channel A start and Channel B stop
common mode:	Channel A start and stop
Input Characteristics:	Channel A and B same as described in Frequency Ratio Mode
Display:	μsec, msec, sec

SCALING	
Frequency Range:	0 to 150 MHz
Scaling Range:	10 to 10^{10} selectable in decade steps

FREQUENCY RATIO MEASUREMENTS	
Frequency Range:	
Input F_A	0 to 150 MHz
Input F_B	0 to 10 MHz
Ratio Range:	10^{-8} to 10^8 (10^9 sec with option 004)
Multiplier:	F_B scaled by 1 to 10^9 selectable in decade steps
Accuracy:	±1 count of F_A ± trigger error of F_B / multiplier
Display:	Dimensionless

$$*\text{Trigger error} < \frac{0.0025\ \mu\text{sec}}{\text{Signal Slope V}/\mu\text{sec}}$$

SPECIFICATIONS continued

PERIOD MEASUREMENTS	
Range:	100 nsec to 10^9 sec (10^{10} sec with option 004)
Resolution:	100 nsec
Accuracy:	±1 count ±reference error ±trigger error**
Input:	Channel A
Display:	μsec, msec, and sec

PERIOD AVERAGE	
Range:	100 nsec to 10 sec (100 sec with option 004)
Accuracy:	$\pm 1 \text{ count} \pm \text{reference error} \pm \frac{\text{trigger error}^{**}}{\text{No. of periods averaged}}$
Input:	Channel A
Periods Averaged:	1 to 10^8 selectable in decade steps
Display:	nsec, μsec, msec

TOTALIZE MEASUREMENTS	
Frequency Range:	0 to 150 MHz
Count Range:	0 to 10^8 (10^9 sec with option 004)
Accuracy:	±1 count

GENERAL SPECIFICATIONS	
Internal Reference Oscillator Characteristics:	
Aging Rate:	$<3 \times 10^{-7}$ per month
Temperature Stability:	$\pm 2.5 \times 10^{-6}$, 0°C to + 50°C
Voltage Stability:	$\pm 1 \times 10^{-7}$, with 10% line voltage variation
Time Base:	.01 Hz to 10 MHz selectable in decade steps
Output:	10 MHz square wave, buffered, TTL compatible
External Reference:	5 or 10 MHz 1V rms into 1 kilohm; selectable by internal/external switch
Marker Output:	Negative-going pulse, 15 volt amplitude, rear BNC, duration equal to channel A trigger point to channel B trigger point
Display:	Long-life digital display tubes; 8 standard, 9 optional (option 004)
Input/Output Connectors:	BNC
Operating Temperature:	0° to 50°C
Line Voltage:	50 Hz to 400 Hz; 115V ± 10%
Power Requirement:	60 watts maximum
Weight:	Net, 15 pounds; shipping, 20 pounds
Dimensions: (HxWxD)	3-15/32 x 16-3/4 x 14 inches; 88 x 425 x 356 millimeters

**Trigger error $\leq \frac{0.3}{(S/N)Fa}$

where S/N equals signal to noise ratio and Fa equals frequency.

SPECIFICATIONS continued

OSCILLATOR OPTIONS

	Option 050	Option 200
Aging Rate/day:	–	$1x10^{-9}$
Aging Rate/month:	$1x10^{-7}$	$3x10^{-8}$
Temperature Stability, 0^{o} to $50^{o}C$:	$\pm 5x10^{-7}$	$\pm 5x10^{-9}$
±10% line voltage stability:	$\pm 5x10^{-8}$	$\pm 5x10^{-9}$
Warmup*:	1 hour	72 hours

*Time to reach aging specification after 24 hours off.

SYSTEMS INTERFACE (Optional on All Models)

Programming Inputs:	
Single Line Commands:	Function, time base, external gate, +/– slope, hold, reset
Logic Levels:	Low TTL level or contact closure to ground for single line commands, inputs are TTL gates
Analog:	Supply ±10V into 10 kilohm to set desired level; accuracy is ±5% of input range
Electrical Outputs:	
Binary Coded Data:	1-2-4-8 code, each data digit
Single Line Signals:	Print, units, decimal point
Logic Levels:	Positive true, from standard TTL integrated circuits

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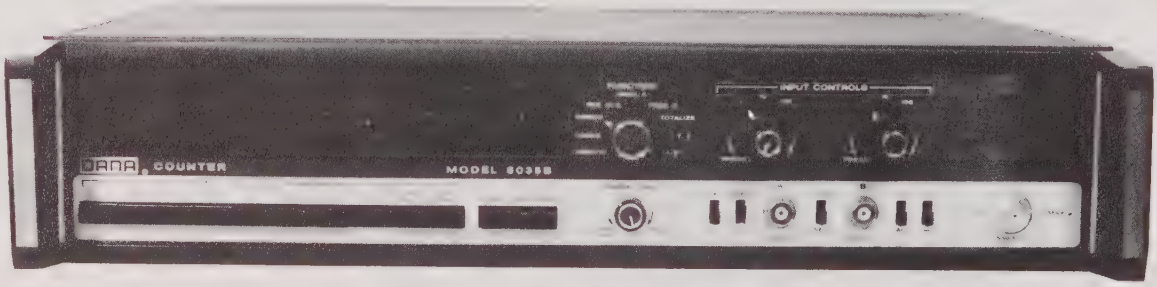


8035B

Figure 1.1 - Models 8015B and 8035B

SECTION 1 GENERAL DESCRIPTION

1.1 SCOPE.

1.2 This manual contains installation, operation, and maintenance instructions for the Dana Models 8015B and 8035B electronic counters (figure 1.1). Both models and optional features are covered; therefore, all descriptions may not apply to a particular instrument.

1.3 GENERAL DESCRIPTION.

1.4 Each model in the 8000B Series is self-contained for its intended range of applications. No external or plug-in accessories are required. Both models have a minimum of six measurement modes: Frequency, Period, Multiple Period Average, Totalize, Time Interval, and Ratio. Both models operate at frequencies up to 150 MHz. Model 8035B operates at RF frequencies. The capability of each model is shown in table 1.1.

1.5 An eight digit display and a high stability reference oscillator provides the standard counter with capability to make meaningful frequency measurements to an accuracy up to 1 part in 10^8. For more demanding applications, a nine digit display and correspondingly higher stability reference oscillators, are available as options.

1.6 The standard temperature compensated crystal oscillator (TCXO) in the counter serves as an ideal reference in a general purpose counter. The average aging rate is 3×10^{-7} per month. Since no temperature controlled oven is used, extended warmup times are not required when moving the counter from one location to another.

1.7 Time Interval Measurements.

1.8 The use of low noise FET input circuitry provides 50 millivolt sensitivity to 100 MHz with a constant 1 megohm input impedance on both the start and stop input channels. The input circuitry includes a three-position attenuator and controls for: trigger level, slope, and coupling, so that triggering can be optimized for non-sinusoidal waveforms.

1.9 Because of high stability input amplifiers, trigger levels will drift less than 5% of full scale over a 10^{o}C temperature range and 200 hours of operating time after initial setting. Frequency adjustments to the counter are not necessary during the instrument warmup period or when changes in temperature occur.

1.10 While making a time interval measurement, it is often useful to observe the waveform under test with an oscilloscope. The counter's marker output may be connected to most oscilloscopes to provide a continuous brightening of that portion of the waveform between the start measurement point and the stop point.

1.11 Time Interval resolution of the counters is 10 nanoseconds. Two independent channels determine the start and finish of the measurement. This permits the line between events occurring in different circuits to be measured. Pulse width and rise time on a non-repetitive waveform can be measured to 10 nanoseconds resolution.

1.12 Two analog outputs are provided on all models with time interval capability for accurately monitoring trigger level settings. The 50% point and 10% - 90% rise time points can be set accurately by measuring the analog voltage outputs with a digital voltmeter.

Table 1.1 - Measurement Capability

Model	Totalize	Period	Period Average	Freq to 150 MHz	Freq to 550 MHz	Ratio	Time Interval
8015B	X	X	X	X		X	X
8035B	X	X	X	X	X	X	X

1.13 RF Measurements.

1.14 Model 8035B has RF measurement capability. The counter features RF amplifiers capable of meaningful measurements as low as 50 mV with the standard prescaler, or as low as 1 mV (–47 dBm) with an optional prescaler (Option 030). Low level, RF signals can therefore be measured without external amplification.

1.15 To measure frequencies between 1 and 550 MHz, the operator simply connects the unknown signal to the input and reads the result. By using a prescaler, both the need for manual tuning and possibility of an incorrect setting have been eliminated. Triggering is automatically optimized for input signal amplitude from 50 millivolts to one volt with the standard prescaler, or from 1 mV to 1 volt with an optional prescaler.

1.16 A wide-band automatic gain control, coupled with excellent sensitivity, enable the carrier frequency of an amplitude modulated signal to be measured. Full accuracy is maintained with greater than 90% amplitude modulation (99% with optional prescaler). Frequency modulated carriers can also be measured as long as the frequency components are within the 1 to 550 MHz bandwidth.

1.17 Model 8035B is equipped with a 550 MHz prescaler. The prescaler maintains the stability and accuracy of the basic 150 MHz counter at radio frequencies. Only 40 milliseconds are required to measure 550 MHz to a resolution of 2 parts in 10^{-7}. This fast measurement time is due to the prescaler's capability to divide the input signal and multiply the measurement time by four.

1.18 OPTIONS.

1.19 All options on the 8000B Series counters should be ordered at the time of purchase. However, the Option 030 RF prescaler (1 mV sensitivity, 10 MHz to 500 MHz) and the Rack Mount Adaptor may be added at anytime.

1.20 Rack Mounting Adapters, Option 003.

1.21 Rack mounting adapters are used where the instrument is to be installed in a relay-rack or cabinet.

1.22 Ninth-Digit Readout, Option 004.

1.23 The 9th Digit Readout adds one more digit to the eight digit counter. The 9th Digit increases the accuracy to 1 part in 10^9.

1.24 Systems Interface, Option 008 (Table 1.2)

1.25 The systems interface, which includes BCD output and remote programming input, is available for all counters.

Table 1.2 - Control Lines

Control	Programming
Function	Single line
Time base	Single line
Stop/Start	Single line
+/– Slope	Single line
Hold/Reset	Single line
Trigger level	Analog voltage

1.26 All remote programming and BCD outputs are compatible with TTL Logic Levels. This allows the series 8000B counters to be interfaced directly to control and recording devices without requiring level shifting and buffer circuitry.

1.27 Rear Input, Option 010.

1.28 The Rear Input provides the user a rear-panel connector for Frequency A, Frequency B, and Frequency C (not in Model 8015B) input signals. The Rear Input option reduces the sensitivity of Frequency A 10 dB above 50 MHz.

1.29 Prescaler (1 mV Sensitivity, 10 MHz to 500 MHz), Option 030.

1.30 The Option 030 Prescaler is available to replace the standard Prescaler. It provides sensitivity as low as 1 mV (–47 dBm). Maximum usable input is 1 volt rms and 5V rms without damage to the prescaler.

1.31 TCXO, Option 050.

1.32 The Option 050 Temperature-Compensated Crystal Oscillator offers a lower aging rate per month, and better voltage and temperature stability than the standard TCXO oscillator.

1.33 Oven Oscillator, Option 200.

1.34 The Option 200 oven oscillator provides an ultra-stable timebase – extending the time between calibrations and serving as a secondary frequency standard. The oven oscillator is in continuous operation whenever the counter is attached to the power line.

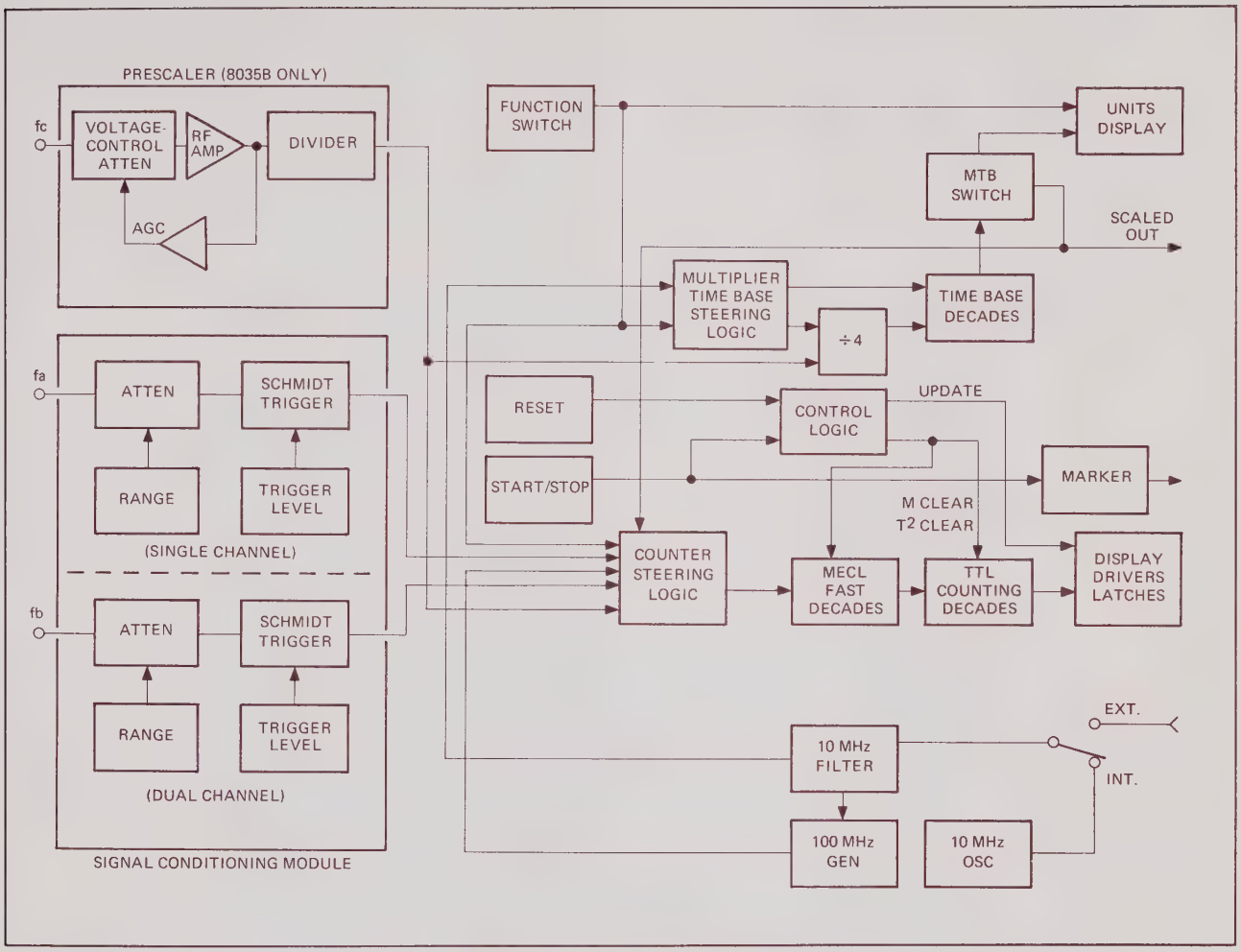


Figure 1.2 - Block Diagram

1.35 ELECTRICAL DESCRIPTION.

1.36 A basic block diagram of the instrument is shown in figure 1.2. Input channels A and B are identical through the attenuator and signal conditioning amplifiers. The input is routed through the BNC input connectors and through the AC/DC coupling switch to the attenuator. The attenuator has three positions: X1 range, X10 range, and X100 range. The attenuator output is applied to the signal conditioning amplifier through an overload circuit that protects the circuitry if an "overload" voltage is applied.

1.37 The signal conditioning amplifier is a low-drift dc-coupled Schmitt trigger circuit. Any point on the input waveform can be selected to trigger the Schmitt circuit by front panel controls: the +/– switch selects either positive or negative slope and the INPUT CONTROLS select the amplitude. Output pulses generated by the Schmitt trigger circuit are applied to the Steering Logic and to the Marker Generator.

1.38 The Marker circuit provides a marker pulse used to intensity-modulate an oscilloscope display. It starts when channel A triggers and terminates when channel B triggers. The pulse represents a precise measurement of the time between channel A and channel B. The oscilloscope trace displays the point where the time measurement starts and terminates. The trigger levels can be adjusted very accurately with the use of the oscilloscope.

1.39 Frequency C (except in Model 8015B) is applied directly to the Prescaler that contains a voltage-controlled attenuator (VCA), RF amplifier, and two high frequency divide-by-two circuits. The dividers scale the input frequency by a factor of four. This is necessary to reduce the frequency to that acceptable by the ECL logic. The voltage-controlled attenuator and RF amplifiers combine to provide automatic ranging over input amplitude variations of 60 dB throughout the operating frequency.

Table 1.3 - Logic Functions of Multiplier Timebase (M/TB) Per Mode

Mode of Operation	Function of MTB switches
Frequency A	Selects gate time
Frequency C	Selects gate time
Period	Selects reference frequency to be counted
Period Average	Selects number of periods to be averaged
Time Interval	Selects the reference frequency to be counted during the time interval A to B
Totalize	Selects the scaling factor of the input frequency
Ratio A/B	Selects number of periods of channel B input to be used as the gate time
Check	Selects gate time

1.40 Reference Conditioning receives a reference frequency from either the internal reference oscillator or from the External Reference input. External reference inputs of 5 MHz or 10 MHz are buffered, amplified, and applied to a Schmitt trigger circuit to produce harmonics at 10 MHz. A filter rejects frequencies other than 10 MHz. The reference signal is passed on to the digital logic section and a 100 MHz Harmonic Generator.

1.41 The counting and multiplier timebase steering logic routes the inputs to the proper set of decades corresponding to the selected operating mode of the instrument. It "steers" the inputs upon commands from the FUNCTION switch.

1.42 Signals to the Control Logic Section are generated by logic in the following blocks in figure 1.2: Multiplier/Timebase (M/TB) Decades and Start/Stop Logic. The M/TB Decades consist of eight TTL decade counters which, together with Start/Stop Logic, inputs from the Steering Logic, M/TB switches on front panel, and the function switch, control operation of the Control Logic. The circuits combine to perform the functions listed in table 1.3 for each operating mode. The M/TB Decades supply a scaled output to a rear panel connector in the Totalize mode. The output is 1/10N x input frequency, where N is the Multiplier setting on the front panel.

1.43 The M/TB switch and the FUNCTION switch operates in conjunction with the Decimal Point Logic and Units Logic to provide proper annunciators and decimal point locations. They also control other logic contributing to the functions listed in table 1.3.

1.44 Timing of the counter is governed by the Control Logic. After the counter is "armed", it opens the Gate upon command of the Start/Stop Logic. After the Gate goes low, two additional pulses are generated: a Prop-Delay (proper delay) pulse and a Display Time pulse. The Prop-Delay allows for settling time of the accumulated count in the counter decades before Update and Print commands are generated. The Display Time pulse, with width determined by the front panel DISPLAY TIME control, controls the length of time that the accumulated count is displayed before the decades are cleared in preparation for a new count.

1.45 The DISPLAY TIME control on the front panel performs three functions. The CCW position removes power from the display tubes and disables the $\pm$18V and +5V supplies. The CW position HOLD allows the meter to hold a measured count indefinitely. Mid-range of the control provides a continuously variable sample rate from 30 msec to over 5 seconds.

1.46 The STORAGE Switch is a two-position switch (storage-off, storage-on) located on the rear panel. When the switch is in the ON position, the display is continuous and changes only when the measurement is different from that counted during the previous measurement cycle. The OFF position disables the display storage so that the accumulation of the count can be observed by the operator. The RESET switch on the front panel enables the operator to start a new measurement cycle.

1.47 The START/STOP switch on the front panel manually generates the Start/Stop commands to the main gate. This switch is used in Totalize mode.

1.48 The Readout assembly is made up of eight in-line display devices with decimal inputs, five annunciator lamps and a main gate annunciator. The count is displayed by the display devices with correctly positioned decimal points and annunciator indicators (nsec, μsec, sec, KHz, and MHz). The gate annunciator indicates the opening and closing of the main gate.

1.49 The counting decades consist of one high-speed decade made up of ECL (emitter-coupled-logic) and seven TTL decade counters. Each decade applies the accumulated count data in BCD format to the Latches and Drivers. The latches are D-type flip-flops which can store a count for a indefinite period of time. When the STORAGE switch is on, the display is continuous and changes only when the measurement is different from that counted during the previous measurement time. The drivers are BCD-to-ten-line decoders that provide a decoded decimal output to light the corresponding numeral on the readout tube.

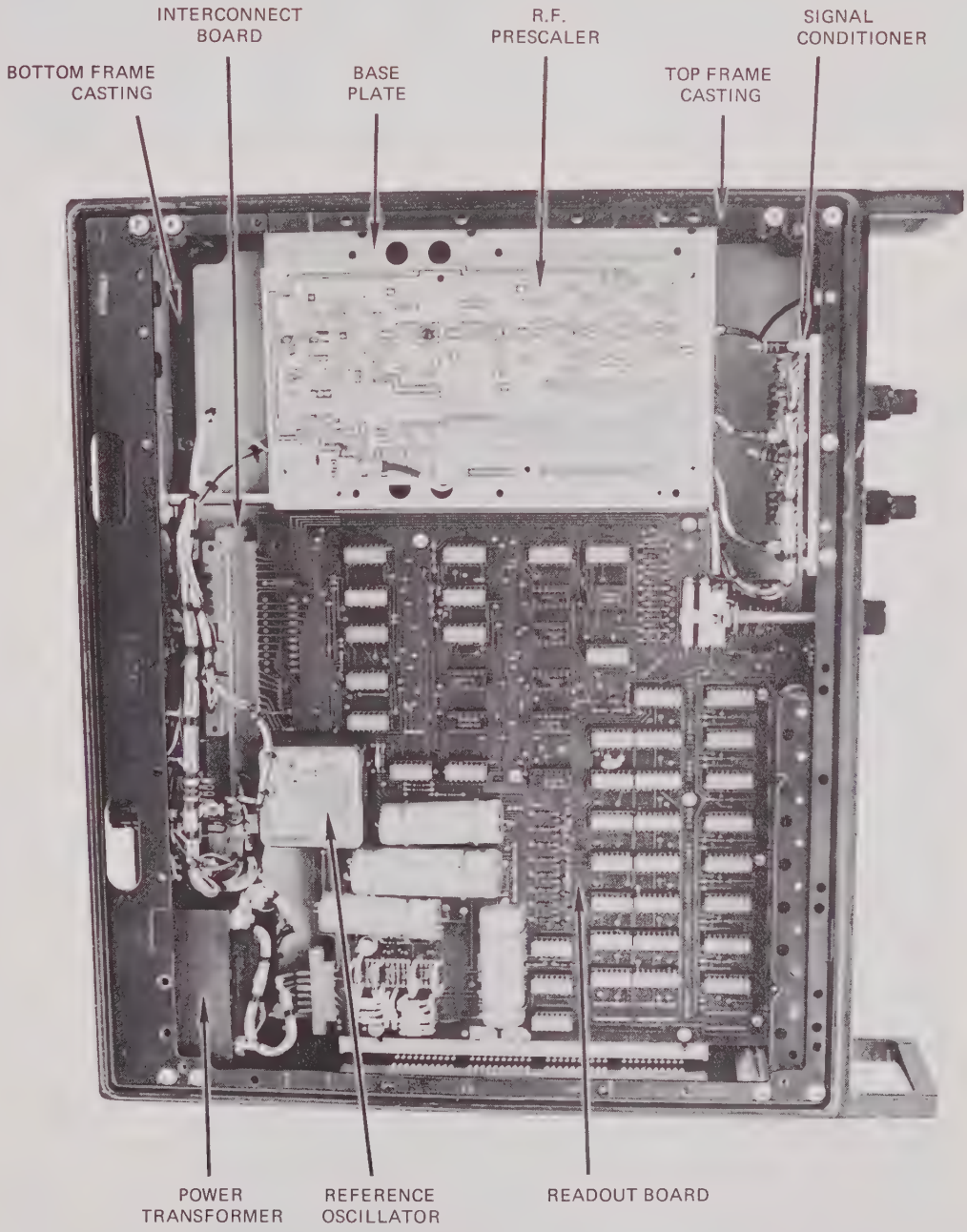


Figure 1.3 - Top View

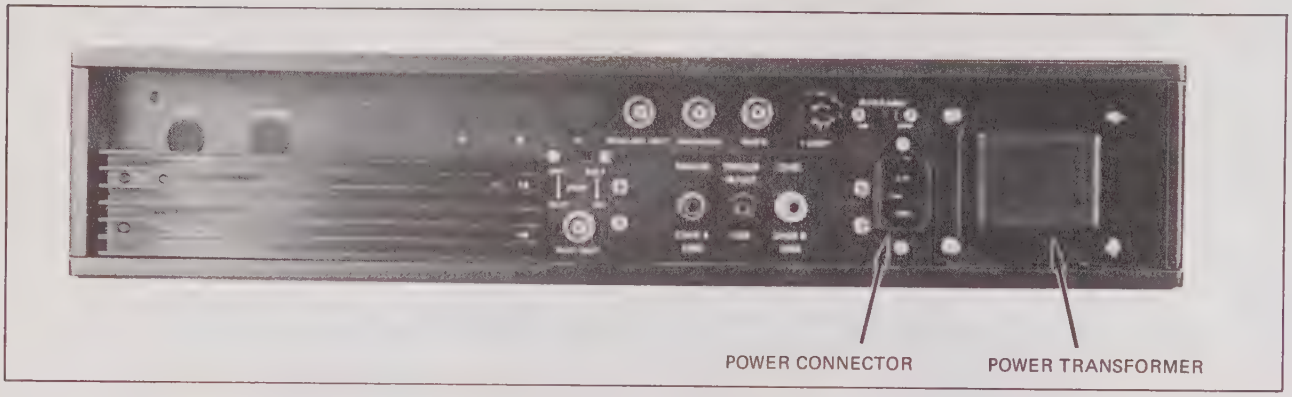


Figure 1.4 - Rear Panel

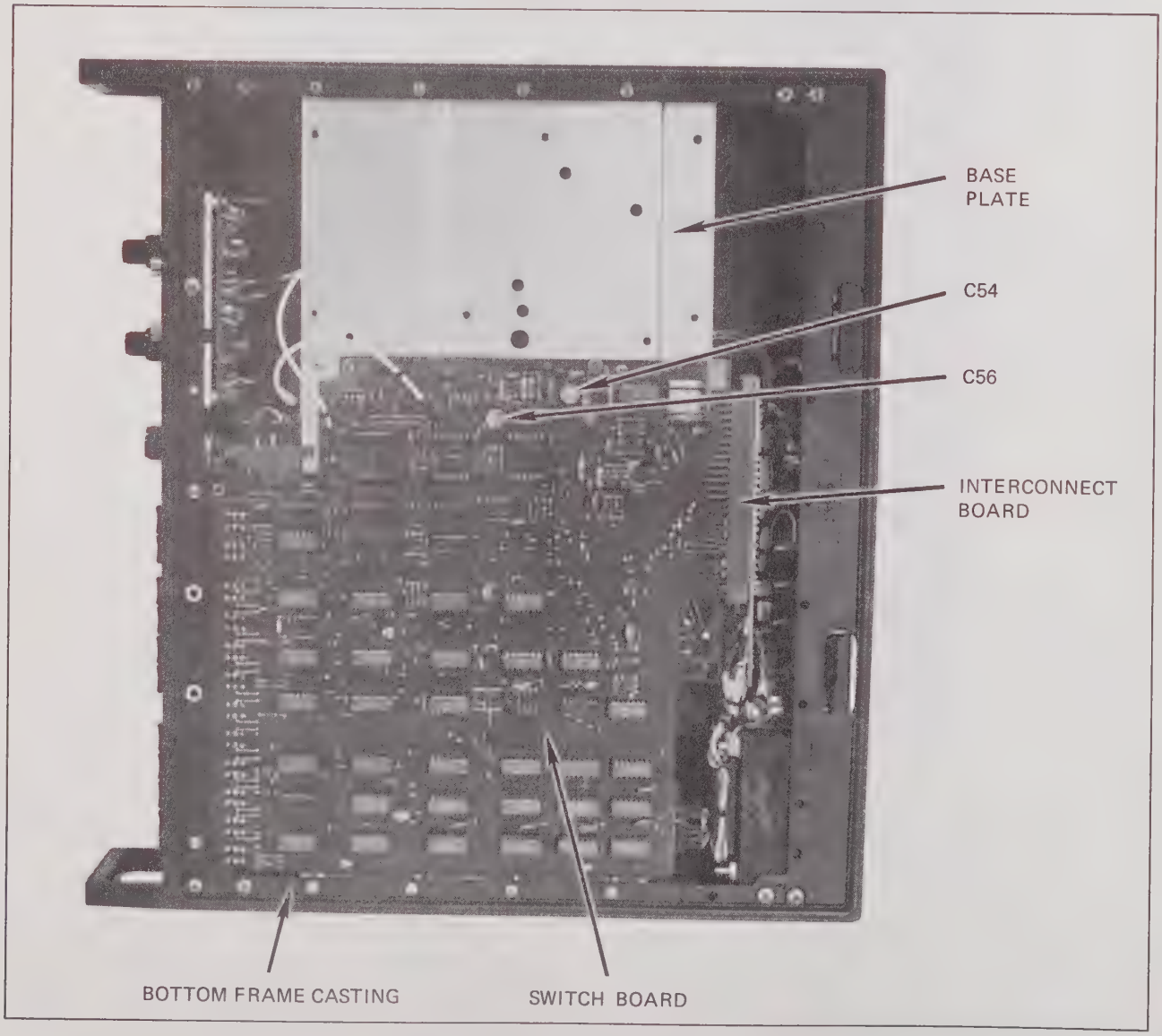


Figure 1.5 - Bottom View

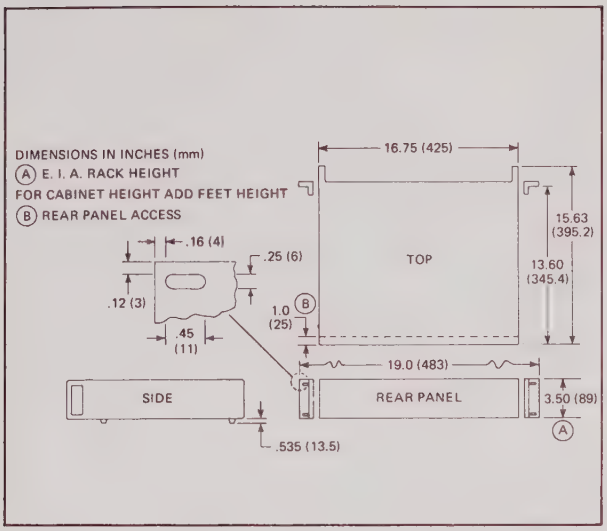


Figure 1.6 - Dimensions

1.50 MECHANICAL DESCRIPTION.

1.51 A top view of the counter is shown in figure 1.3. The counter shown (8035B) is equipped with the RF prescaler mounted on the base plate. The Readout board is mounted on the top of the base plate. The Interconnect board connects the Readout board and the Switch board together electrically at the rear of the Readout and Switch board. The signal conditioner is attached to the front panel. The power transformer and rear panel are one assembly. The rear panel (figure 1.4) assembly is clamped between the top and bottom frame castings.

1.52 The bottom view of the counter is shown in figure 1.5. The Switch board is mounted on the base plate. The base plate is attached to the bottom frame casting.

1.53 A dimensional outline of the 8000B series counter is shown in figure 1.6.

2.1 UNPACKING AND INSPECTION

2.2 The Series 8000B Counter is packed in a molded plastic-foam form within a cardboard carton for shipment. The plastic form holds the Counter securely in the carton and absorbs any reasonable external shock normally encountered in transit. Prior to unpacking, examine the exterior of the shipping carton for any signs of damage. Carefully remove the Counter from the carton and inspect the exterior of the instrument for any signs of damage. If damage is found, notify the carrier immediately.

2.3 Included with the Counter packed in the container are the instruction manual, Dana Part Number 980448, and power cord 403530. Counters which are equipped with remote programming and BCD output (Option 008 systems interface) are shipped with three mating connectors, 600698, and keys included.

2.4 BENCH OPERATION.

2.5 Each Counter is equipped with a tilt bail or "kickstand" to enable the front of the instrument to be elevated for convenient bench use. The tilt bail is attached to the two front supporting "feet" at the bottom of the instrument. For use, the bail is pulled down to its supporting position.

2.6 RACK MOUNTING.

2.7 The instrument can be mounted in a standard 19-inch rack with the optional rack-mounting flanges (403402, includes attaching hardware). To install the flanges, proceed as follows:

a. With instrument on its side, remove four Phillips-head screws holding bottom cover. Remove cover. Remove screws holding feet (and bail) in place. Replace bottom cover.

b. Place one of the supplied screws through each of the two holes in the mounting flange (figure 2.1). Thread a securing nut onto each screw just enough to attach it to the screw (approximately one turn).

c. Place the mounting flange onto the mounting slot in the instrument side panel so that the securing nuts fit entirely into the slot. Be sure the rack-mount slots on the flange are toward the front of the instrument.

d. Tighten screws. The securing nuts will rotate and hold the flange securely in place.

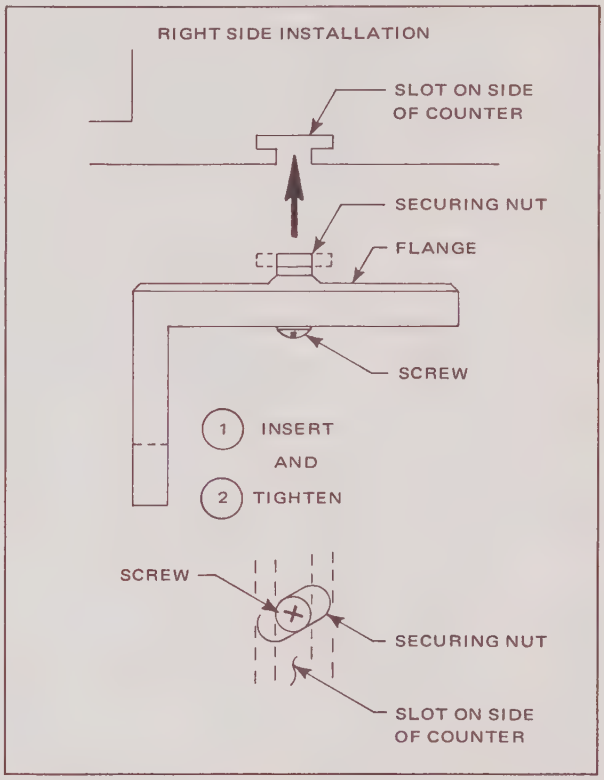


Figure 2.1 - Rack Mount Installation

2.8 POWER CONNECTIONS.

2.9 Power requirements for domestic units are 115V ± 10%, 50 to 400 Hz. Power consumption is 60 watts maximum. All 8000B series counters are adaptable for 230V operation. Figure 2.2 shows input wiring for 230V ± 10% line voltage.

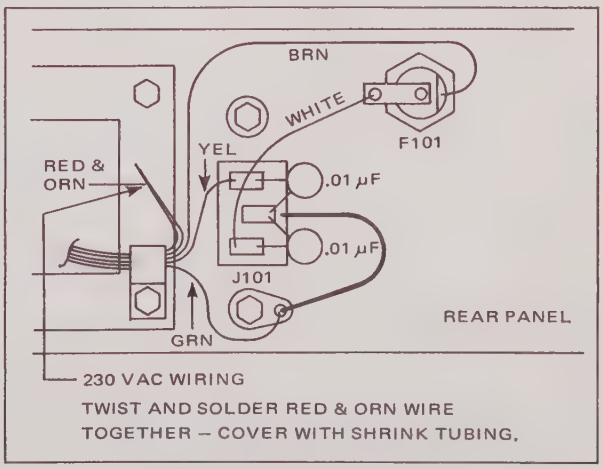
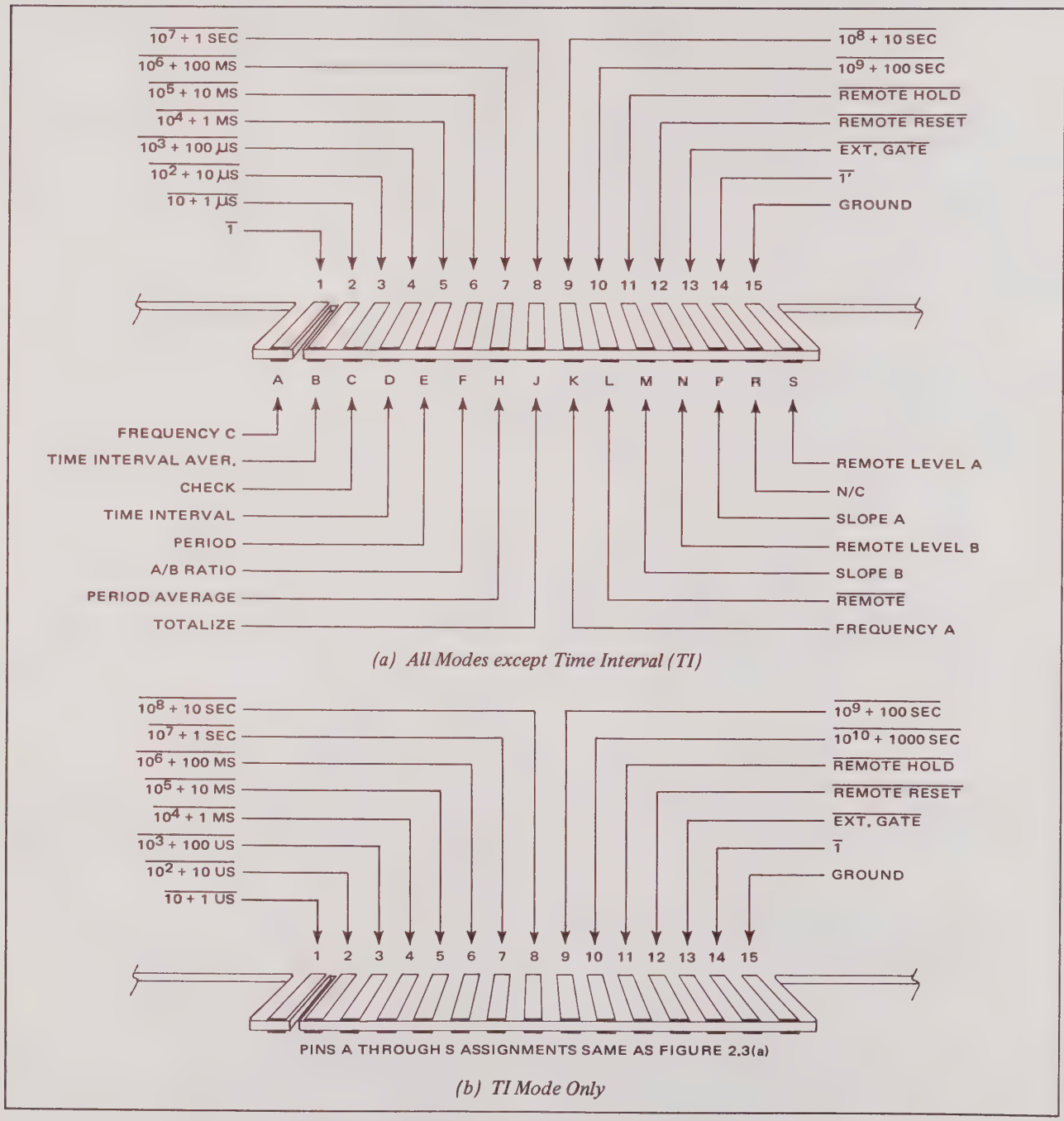


Figure 2.2 - 230V Operation



(a) All Modes except Time Interval (TI)

(b) TI Mode Only

Figure 2.3 - REMOTE Connector J110 Pin Assignments

2.10 Power Cable.

2.11 A standard power cable having a three-pin plug is supplied with the counter. The cord connects to the power connector J101. The ground pin (round) is attached to the main frame of the counter. It is important that this pin be connected to a good quality earth ground.

2.12 Fuse.

2.13 The power fuse holder is located on the rear panel of the counter. A .75 amp 3AG fuse is used.

2.14 REMOTE PROGRAMMING AND BCD OUTPUT.

2.15 Remote Programming.

2.16 Remote programming commands are received through the REMOTE connector J110 located on the rear panel. Commands are generated by a closure to $\overline{\text{Remote}}$, J110 pin L. Pin assignments of J110 are listed in figure 2.3a except when operating in the Time Interval mode. Pin assignments for TI mode are shown in figure 2.3b. J110 is keyed between pins 1 and 2. Typical programming timing is shown in figure 2.4. Programming requirements are as follows:

a. Output of programmer must be able to withstand a back bias of ≥ 5 volts.

b. Low must be $\leq .2$ volts.

c. Output of programmer must be able to sink 16 milliamps.

2.17 FUNCTION.

2.18 Pins A through K of J110 are the input lines corresponding to the FUNCTION switch on the front panel. Note that the function lines are the complements of the corresponding function as indicated by a bar over the name. For example: with FREQ A function selected the line marked Freq A or Fa should be low ($\overline{\text{Fa}}$). To remotely program any of the operating modes, the front panel FUNCTION switch must be in the REMOTE position. The function is then programmed by a closure to J110 - pin L from the appropriate pin. Settling time for the Function lines are 100 ns.

2.19 MULTIPLIER TIME BASE.

2.20 Pins 1 through 10 of J110 are lines corresponding to each of the MULTIPLIER/TIMEBASE pushbutton switches except when operating in the Time Interval mode (see figure 2.3b). Settling time for the Multiplier Time Base lines is 100 ns.

2.21 INPUT CONTROLS.

2.22 The INPUT CONTROLS and the "+/–" slope switch on the front panel are duplicated by lines on pins M through S of J110. For Remote Programming of these input controls, the trigger level for input A and B must be in the PRESET position. The channel A trigger level is then controlled by the voltage applied to J110, pin S; channel B trigger level is controlled by the voltage applied to pin N. The value of the external trigger level voltage applied to pins S and N can be calculated according to the following formula.

$$Vp = 10\left(\frac{TL}{R}\right)$$

Where: Vp = external trigger level voltage

TL = desired trigger level

R = Input voltage range

Example 1: To obtain a trigger level of .7 volts on the 1 volt range.

$$Vp = 10\frac{.7}{1} = 7 \text{ volts to pin S or N}$$

Example 2: To obtain a trigger level of –50 volts on the 100-volt range.

$$Vp = 10\frac{-50}{100} = -5 \text{ volts}$$

2.23 Both positive and negative trigger levels may be programmed into pins S or N. Settling time is 1 microsecond for the trigger level up to ± 300% of the input range.

2.24 SLOPE.

2.25 The counter triggers on the positive slope unless there is a closure from pin M to pin L for channel B slope or (and) pin P to pin L for channel A slope. With a closure, a negative slope is programmed. Settling time is less than 1 microsecond.

2.26 HOLD.

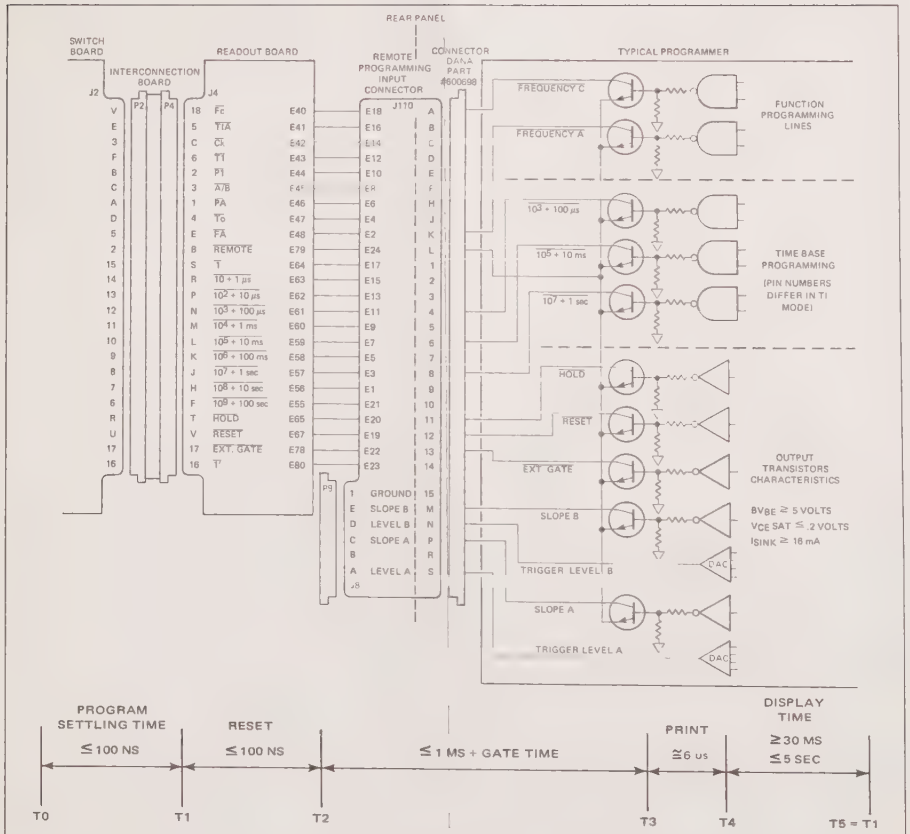
2.27 The Hold line, pin 11 of J110, corresponds to the full clockwise position of the DISPLAY TIME control on the front panel. When the Hold line is low, the counter takes one reading and holds the measurement until the Reset is activated.

2.28 RESET.

2.29 Reset corresponds to the front panel RESET switch. The reset must be held low for a minimum of 100 nanoseconds. The main gate opens in less than 1 millisecond after the positive edge of the reset closure.

2.30 EXTERNAL GATE.

2.31 The external gate line, pin 13 of J110, is used in the Totalize mode to externally establish a gate time during which Frequency A is counted. The external gate must be greater than 100 nanoseconds. Two contact closures are required per gate time or measurement. The gate is initiated in less than 50 nanoseconds after the falling edge of the first



T0	Select function, multiplier time base, slope, trigger level. The following are set internally: units, decimal point and the arm flip-flop.
T0 - T1	Time for inputs to settle ≤100 ns trigger levels 1 μs.
T1 - T2	Reset or external gate time ≤100 ns.
T2 - T3	≤1 ms + gate time, gate opens, counts accumulate in the counter, gate closes, display flip-flop is reset, arm flip-flop cleared and fires a 1 μsec delay for update.
T3 - T4	Print pulse External Hold takes effect if applied.
T4 - T5	Display time times out ≥30 ms to ≤5 sec selectable on front panel.

Figure 2.4 - Typical Programmer and Timing Diagram

contact closure. The next contact closure terminates the gate and holds the accumulated reading. The next external gate continues the count and so on. The count may be cleared by pulling the Reset line low.

2.32 BCD Output.

2.33 BCD outputs of the counter are found on the rear panel connectors J111 and J112. Connector J111 is keyed between pins 2 and 3 and connector J112 is keyed between pins 3 and 4. The data is delivered in a 8-4-2-1 positive true format. The outputs are capable of driving five TTL loads. Outputs are referenced to J112 - pin 14 which is the Zero Reference. The outputs are at TTL logic levels which are:

V_{Low} 0 to +.5V

V_{High} +2.4V to +5.0V

2.34 Figure 2.5 shows the pin assignments of the RECORDER connectors J111 and J112. V1 through V9 represents the corresponding readout "windows" with V1 to the right, the least-significant bit. Each line is identified by its position V1 through V9 followed by its binary weight. For example, a seven in the most-significant bit is shown as:

V9 –8 J112, pin C = 0 – Low

V9 –4 J112, pin B = 1 – High

V9 –2 J112, pin 3 = 1 – High

V9 –1 J112, pin 2 = 1 – High

Data is good at all times except for a 5 microsecond period before the PRINT pulse.

2.35 UNITS.

2.36 Pins D through K of J112 correspond to the annunciators on the readout panel. They identify the units of time or frequency in which the measurement is expressed. The units outputs are at TTL logic levels.

2.37 DECIMAL POINTS.

2.38 Pins 4 through 11 of J112 define the position of the decimal point. The lines DP1 through DP8, indicate the number of places to the left of the least-significant digit at which the decimal point is placed. The decimal outputs are at TTL logic levels.

2.39 PRINT COMMAND.

2.40 The Print Command is a 0 to +5 volt pulse of 6 microsecond duration appearing at J112, pin S. The print pulse indicates that the data is at the output and can be printed.

2.41 ONE REFERENCE.

2.42 The output at J112, pin 15 is One Reference. It is used for some printers which require a reference voltage. The one reference will supply approximately 2.5 volts at less than .1 milliamps.

2.43 OPERATING PROCEDURES.

2.44 Table 2.1 describes the function of each operating control and each connector on the instrument. Tables 2.2 through 2.9 describe procedures for operating the instrument in each of the measurement modes.

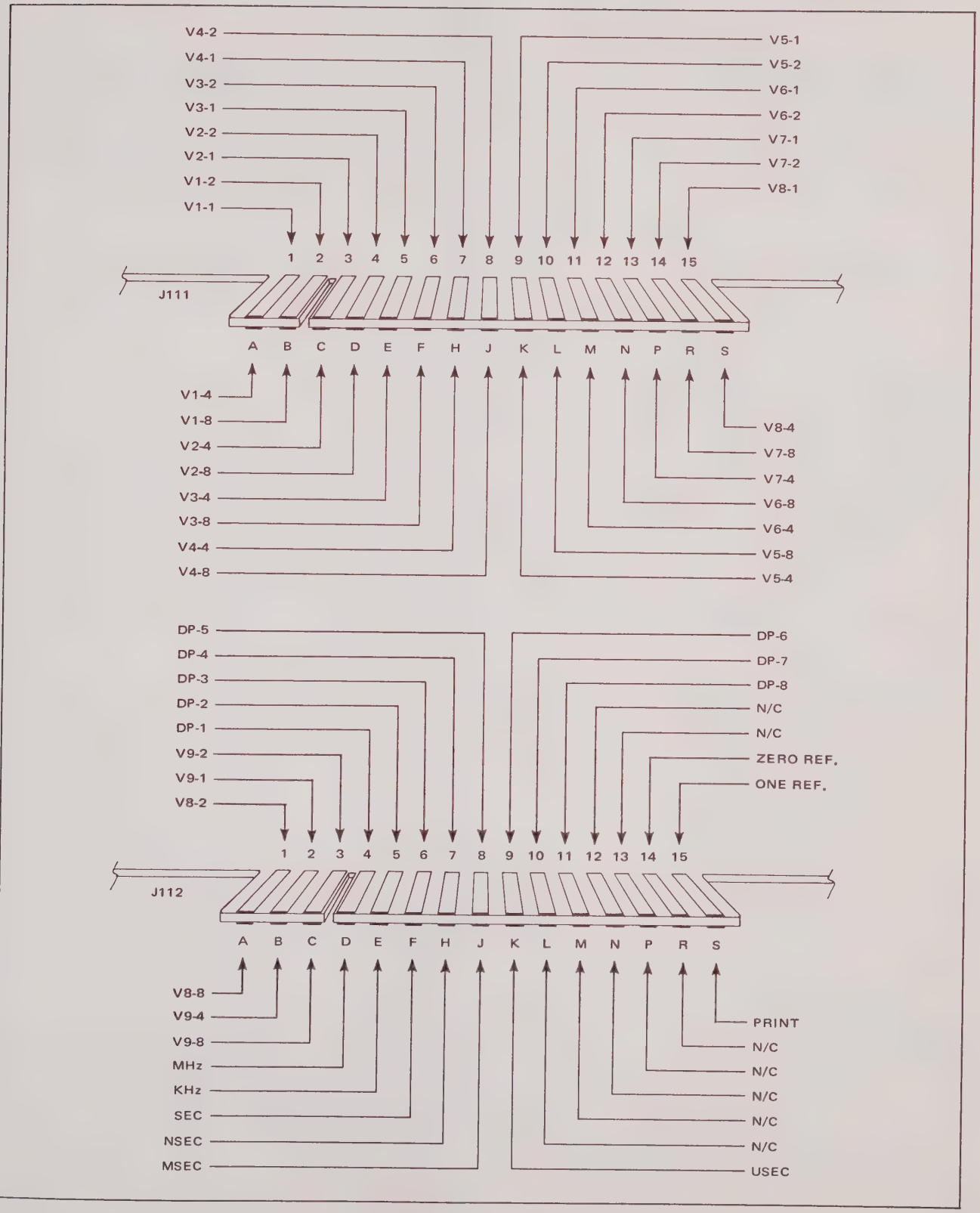


Figure 2.5 - J111 and J112 Recorder Outputs

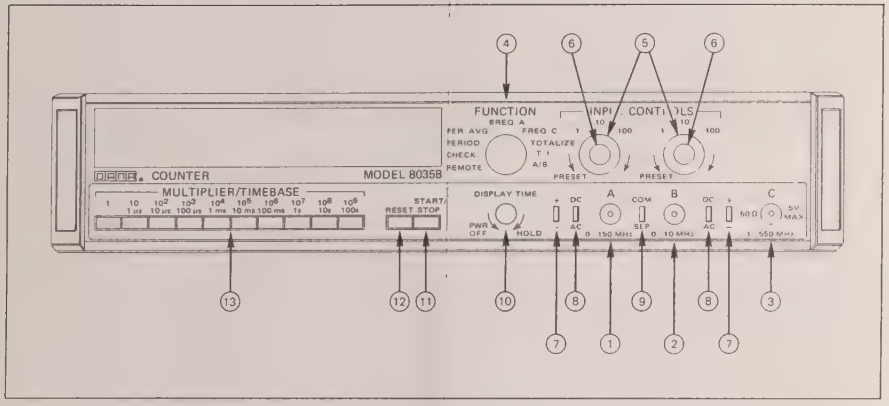


Figure 2.6 - Front Panel

Table 2.1 - Controls and Connectors (see figure 2.6)

input connectors (BNC type)	(1) A INPUT	Used for each function except FREQ C (500 MHz). It accepts up to 250V RMS or 300V peak on all ranges except 150V RMS or 200V peak to 1 MHz on 1V range without damage.
	(2) B INPUT	Always used in conjunction with Channel "A" for making ratio and time interval measurements. It accepts up to 250V RMS or 300V peak on all ranges except 150V RMS or 200V peak to 1 MHz on 1V range without damage.
	(3) C INPUT*	Used in the FREQ C mode only. It accepts frequencies from 1 MHz to 550 MHz and amplitudes from 50 mV to 1V. It accepts a maximum of 5V without damage. This input has no trigger controls because the slope is always set for +; the coupling is always AC; the level is set at the 0 crossing; and the attenuator is automatic.

Control	Position	Action
(4) FUNCTION (rotary switch)	REMOTE	This puts the FUNCTION switch, MULTIPLIER/TIME BASE controls, RESET and START/STOP switches, and the +/– slope switches under remote digital programming control, regardless of what position they are in at the time. The trigger level may be remotely programmed using an analog voltage. To do this, it is necessary for the trigger level control to be set at zero or for the attenuator to be in PRESET. The AC/DC coupling switch, the SEP/COM switch, and the attenuator cannot be programmed.
	CHECK	In this mode, the counter measures its internal 10 MHz reference. The rear panel scaled output provides a TTL squarewave with a frequency equal to 10 MHz divided by the multiplier setting.
	PERIOD	In this mode, the amount of time for one period of the input waveform is measured.
	PER. AVG.	In this mode, a number of input waveform periods are averaged and measured. The number of periods is determined by the multiplier control.
	FREQ A	In this mode, the frequency on the A channel input is measured.
	FREQ C*	In this mode, the frequency on the C channel input is measured.
	TOTALIZE	In this mode, the number of events occurring between the start and stop command is totaled.
	T.I.	In this mode, the time interval between two electrical events is measured. The start point is determined by the A trigger controls and the stop point by the B trigger controls.
	A/B	In this mode, the ratio of the frequency applied at the A input to the frequency applied at the B input is measured.
INPUT CONTROLS		The purpose of the controls is to set the point on the incoming waveform that causes a trigger pulse to be sent to the counting logic. In the frequency mode, it is necessary to send one trigger pulse during each cycle of the input signal; the number of such trigger pulses received during a gate time determines the frequency measured.

*Not in 8015B

Table 2.1 - Controls and Connectors (Continued)

Control	Position	Action
(5) Trigger Range (outer switch)	1	Couples the input signal conditioner directly. Maximum usable signal is ±3 volts peak.
	10	Attenuates the input voltage by ten or 20 dB. Maximum usable signal is ±30 volts peak.
	100	Attenuates the input signal by one hundred or 40 dB. Maximum usable signal is ±300 volts peak.
		The trigger range also adjusts a special circuit that is designed to prevent false counts due to noise superimposed on the waveform being measured. This special circuit is called the trigger hysteresis. When the trigger range is in the 100V range it prevents all false counts due to superimposed noise of amplitude up to 2.5 volts peak to peak. In the 10V range, the protection is 250 mV; in the 1V range, it is 25 mV. It is therefore most desirable to have the range control set to the highest range possible for any given measurement – the higher the range, the greater the hysteresis protection.
(6) Trigger Level (inner control)		The level control provides continuous adjustment of the trigger amplitude from –300% of the trigger range setting to +300%. (If the trigger range control is set on the 10V range, for example, the trigger level control can be adjusted to cause triggering between –30V and +30V.)
	PRESET	When making frequency measurements, the waveform being measured is usually a low amplitude sinewave. Because this waveform is so widely encountered, a PRESET position has been included at which the counter triggers at a point ≤ ±5% of range.
(7) +/– Slope (slide switch)		Selects which slope of the incoming waveform is to trigger the counter (positive or negative).
	"+"	Causes triggering on the positive-going slope.
	"–"	Causes triggering on the negative-going slope.
(8) AC/DC Coupling (slide switch)	DC	Couples the input signal directly to the signal conditioner. Signal conditioner responds to dc signal changes. Used for time interval measurements.
	AC	Couples the input signal via a capacitor. Signal conditioner responds to periodic AC waveforms. Used for Frequency, Period, and Period AC measurements.
(9) COM/SEP (slide switch)	COM	(Common.) Directs the input signal from input A to channel A and channel B. Used for time interval and multiple time interval average measurements.
	SEP	(Separate.) Connects channel A to channel A input and connects channel B to channel B input.

Table 2.1 - Controls and Connectors (Continued)

Control	Position	Action
(10) DISPLAY TIME (rotary control with switch)	PWR OFF	(Power off.) Turns off the output of the +5 volt, and ±18 volt regulators. Turns off the +150 volts to the display tubes.
	DISPLAY TIME	Applies power to all circuits. Provides a 30 ms (CCW) to 5 second (CW) display time interval between measurements.
	HOLD	Programs the counter to take one measurement. Displays and stores that measurement until RESET is depressed or the position of the DISPLAY TIME control is changed.
(11) START/STOP (momentary pushbutton switch)	Depressed momentarily	This switch is used in the totalize mode. When pushed the first time, the counter starts counting; pushed the second time, the counter stops counting and holds the reading.
(12) RESET	Depressed momentarily	Resets the digital counter to all zeros, arms the counter for a new reading. Commands a new reading anytime.
(13) MULTIPLIER/TIME-BASE Switches (pushbutton switches)	Top row of numbers: 1 10 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9	In Period Average and Time Interval Average modes, the numbers represent the multiplier. This indicates the number of periods or time intervals over which the measurement will be averaged. The higher the multiple, the greater the resolution and the slower the measurement time. In Frequency Ratio mode (A/B), the numbers indicate the number of cycles of the channel B (denominator) signals used to make the ratio measurement. The greater the number of cycles, the greater the resolution and the slower the measurement time.
	Lower row of numbers: 1 μs 10 μs 100 μs 1 ms 10 ms 100 ms 1s 10s 100s	In Frequency mode, the numbers select the time base control. This controls the time the internal gate is open. The longer the gate is open, the greater the resolution, and the slower the measurement time. In Period and Time Interval modes, the numbers indicate the reference frequency to be counted during the gate time. The shorter the time base selected, the greater the resolution; therefore, the left most button is usually selected for these operating modes.

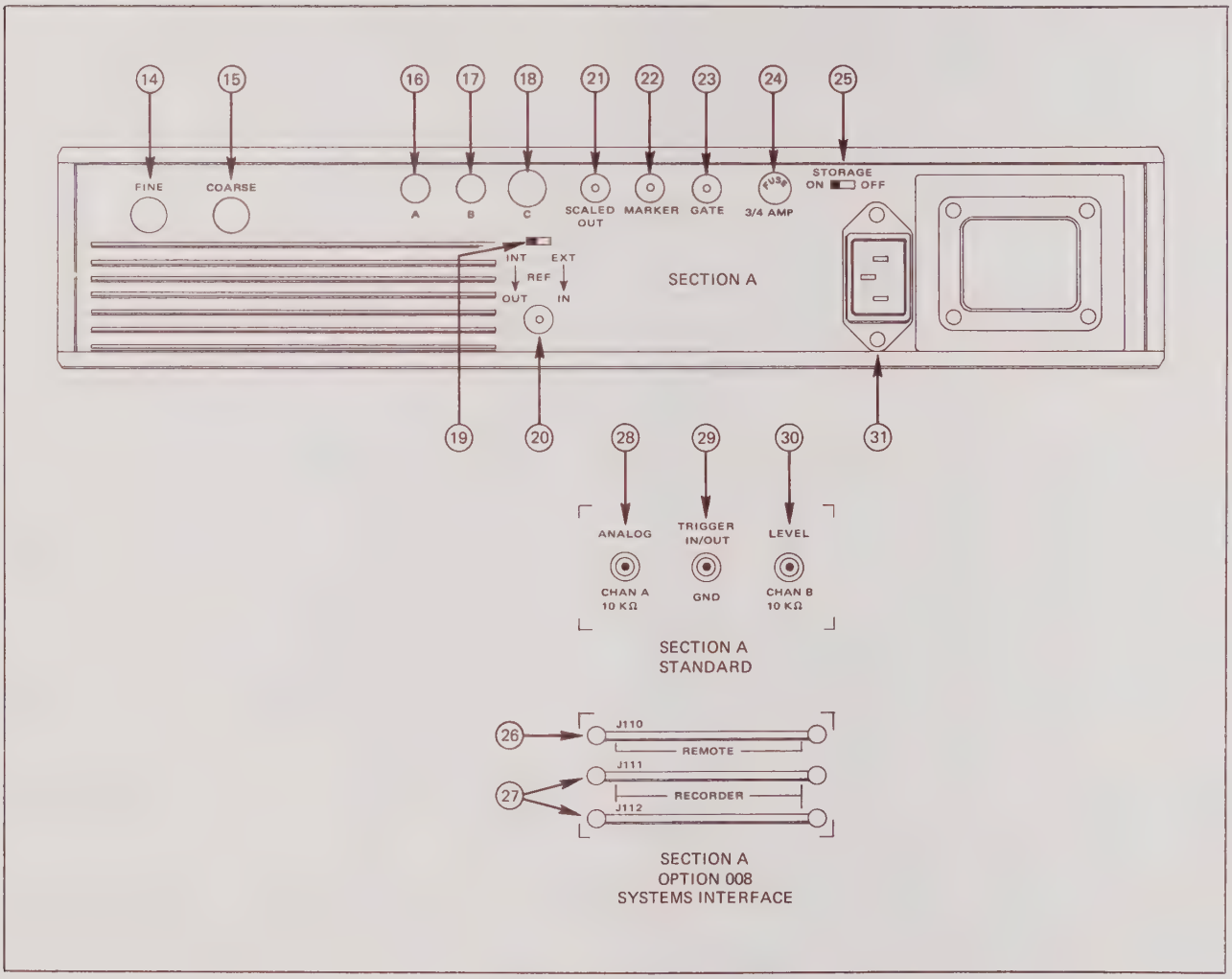


Figure 2.7 - Rear Panel

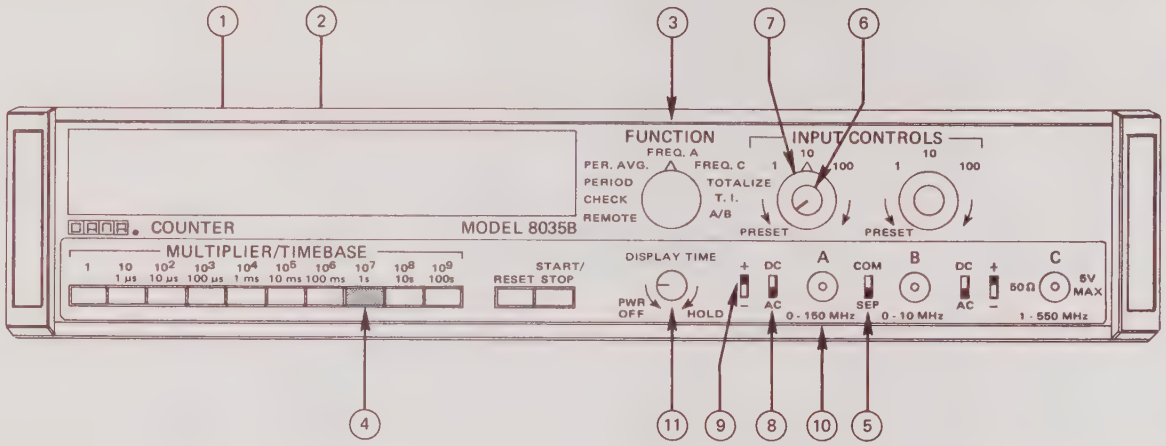
Table 2.1 - Controls and Connectors (Continued)

REAR PANEL (see figure 2.7)

(14) FINE		Access hole used in the FINE adjustment of the ovenized oscillator Option 200. See Calibration.
(15) COARSE		Access hole used in the COARSE adjustment of the ovenized oscillator Option 200. See Calibration.
(16) "A" (BNC connector)		Provides rear input for channel A. Used in Option 010 rear input. Degrades sensitivity by 10 dB above 50 MHz.
(17) "B" (BNC connector)		Provides rear input for channel B. Used in Option 010 rear input.
(18) "C"* (BNC connector)		Provides rear input for channel C. Used with Option 010 rear input.
(19) INT/EXT REF. (slide switch)	INT (Internal)	Routes the internal reference oscillator to the reference filter and to the reference BNC connector.
	EXT (External)	Routes the external reference oscillator from the reference BNC connector to the reference filter circuit.
(20) REF (BNC connector)		Used as internal reference oscillator output when the REF switch is in INT position. Used as external input to reference filter when the switch is in EXT position. The counter will accept 5 and 10 MHz external reference.
(21) SCALED OUT (BNC connector)		Provides a SCALED OUTput of the input in Totalize mode.
(22) MARKER OUT (BNC connector)		Provides a negative 18 volt output starting with trigger A and ending with trigger B. Used to modulate the Z axis of an oscilloscope.
(23) GATE (BNC connector)		Provides a positive true GATE output capable of driving five TTL loads.
(24) FUSE		Provided for the protection of internal circuits in the counter. Located on the rear panel. 3 AG, 3/4 AMP.
(25) STORAGE (slide switch)	OFF	Allows the counter to continuously update the display. Automatically off in the Totalize mode.
	ON	Allows the counter to store information and periodically updates the display.
(26) REMOTE (edge plug)		Provides an input connector to program the counter on models with Systems Interface, Option 008.
(27) RECORDER (edge plug)		Provides two output connectors for data acquisition. Found on models with Systems Interface, Option 008.
(28) ANALOG, CHAN A		Used to measure or program a trigger level to channel A.
(29) TRIGGER IN/OUT GND		Used as a ground return for channel A and B trigger level input and output.
(30) ANALOG, CHAN B		Used to measure or program a trigger level to channel B.
(31) Power Connector		A three pin connector used for power input. Third pin is power ground.

*Not in 8015B

Table 2.2 - Frequency Measurement 0 - 150 MHz

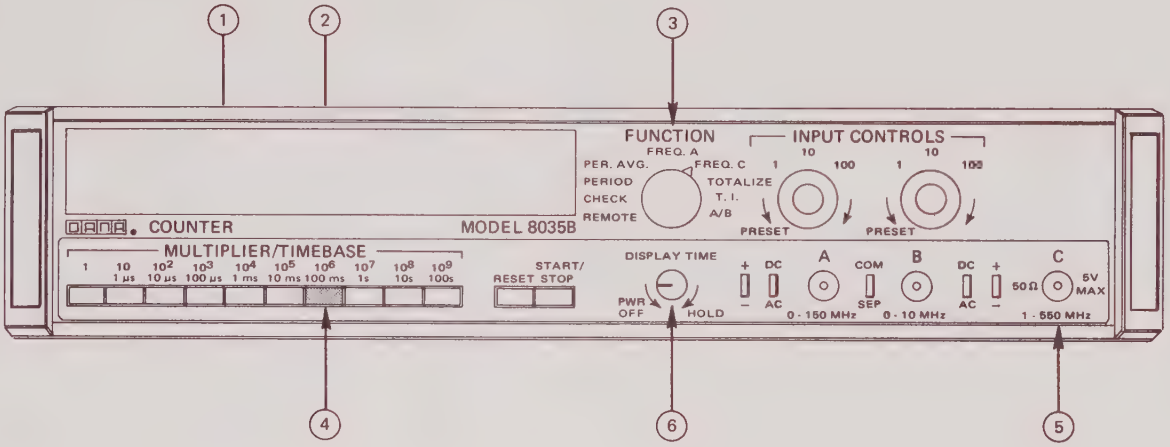


1. Connect AC power.
2. Set STORAGE switch to the ON position.
3. Set the FUNCTION switch to FREQUENCY A.
4. Set the TIMEBASE switch to desired gate time.
5. Set the SEP/COM to SEP.
6. Set channel A level control to desired trigger level or to PRESET to trigger at ≅(0) zero volts.
7. Set INPUT CONTROL range switch to be compatible with the input signal amplitude (1, 10 or 100 volt range).
8. Set AC/DC coupling to AC or DC.
9. Set the A slope to (+) plus.
10. Connect input signal (0 to 150 MHz) to channel A input jack. Note: Max. input 250V RMS or 300V peak.
11. Set DISPLAY TIME to a convenient display interval.

Example: Input frequency to be measured is 600 hertz at 8 volts peak to peak. The TIMEBASE is set to 1 second. Input voltage range is set to 10 volts, trigger level to PRESET, slope to plus and AC/DC to AC. Display will be .000600 MHz with 1 hertz resolution. Change the TIMEBASE to 10 second, the display will be .6000 kHz with 0.1 hertz resolution. Change the TIMEBASE to 100 sec and the display will be .60000 kHz with 0.01 hertz resoltuion.

NOTE: A much faster reading would be to use the PERIOD mode and measure the period of the frequency.

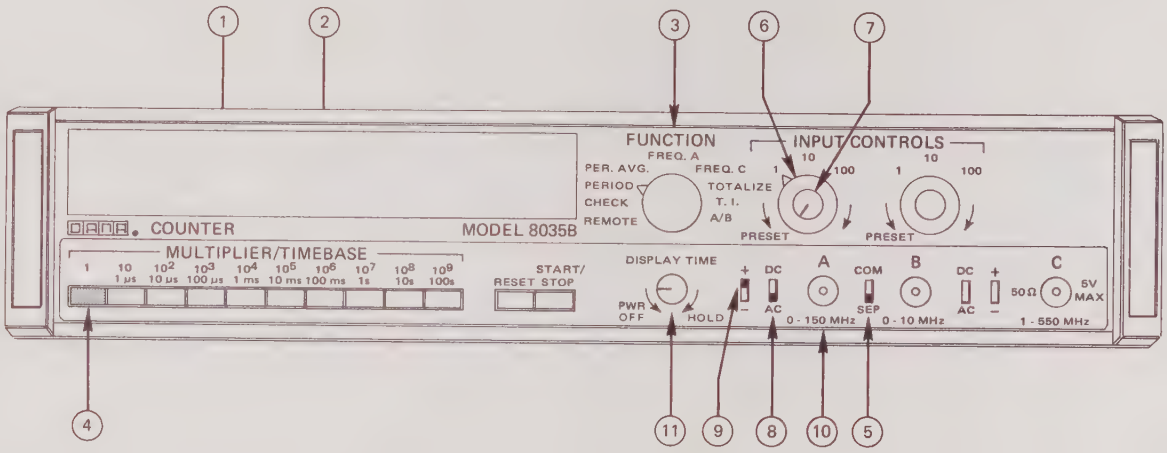
Table 2.3 - Frequency Measurement 1 - 550 MHz (Not in 8015B)



1. Connect AC power.
2. Set STORAGE switch to the ON position.
3. Set the FUNCTION switch to FREQUENCY C.
4. Set the TIMEBASE switch to the desired gate time.
5. Connect the input signal from 1 to 550 MHz (10 to 500 MHz with Option 030) in frequency to channel C input. Note: Max. input operating input is 1V RMS. Max. input without damage is 5V RMS.
6. Set DISPLAY TIME to a convenient display interval.

Example: Input frequency to be measured is 200 MHz at .5V rms. The TIMEBASE is set to 100 milliseconds. The trigger level setting is automatic in the FREQUENCY C function. The display will be 200.00000 MHz with 10 hertz resolution. Gate time is expanded by 4 in this mode of operation (i.e., a 100 ms gate selected on front panel will actually be 400 milliseconds).

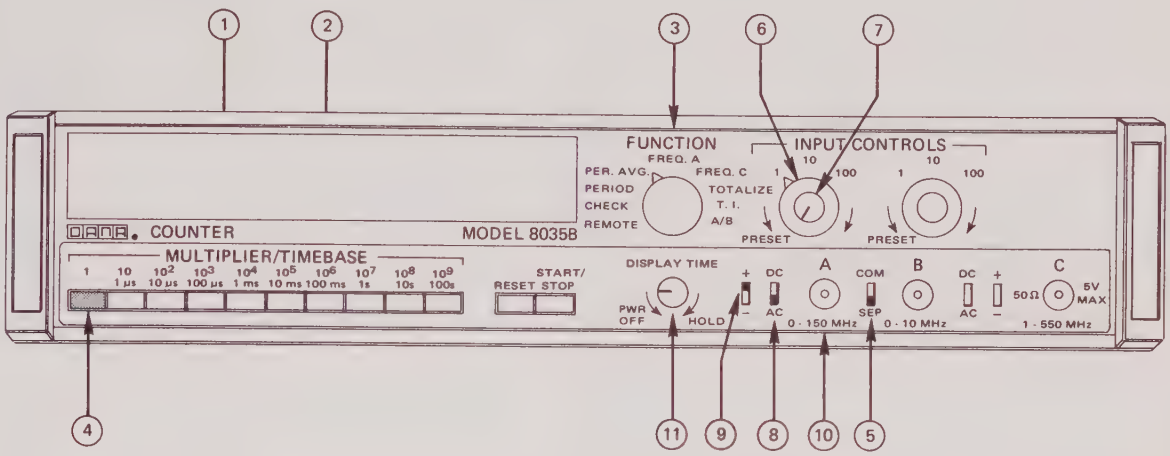
Table 2.4 - Period Measurements



1. Connect AC power.
2. Set STORAGE switch to the ON position.
3. Set the FUNCTION switch to PERIOD.
4. Set the TIMEBASE switch to the desired time units to be counted.
5. Set the SEP/COM to SEP.
6. Set the channel A INPUT CONTROL range switch to be compatible with the input signal amplitude.
7. Set the channel A trigger level control to the desired trigger level or to PRESET to trigger at ≅(0) zero volts.
8. Set the AC/DC coupling to AC or DC on channel A.
9. Set the A slope to (+) plus or (–) minus.
10. Connect the input signal (0 to 10 MHz) to channel A input jack.
11. Set DISPLAY TIME to a convenient display interval.

Example: Input PERIOD to be measured is 1 millisecond at 1V peak. The TIMEBASE is set to 1. The channel A INPUT CONTROL switch is set to the 1-volt range, trigger level is set to the PRESET position and AC/DC is set to AC. The display will be 0001000.0 microseconds with 100 nanoseconds resolution.

Table 2.5 - Period Average Measurements



(1) Connect the AC power.

(2) Set the STORAGE switch to the ON position.

(3) Set the FUNCTION switch to PERIOD AVERAGE.

(4) Set the MULTIPLIER switch to the desired time multiplier position.

(5) Set the SEP/COM switch to SEP.

(6) Set the channel A INPUT CONTROL range switch to match the input signal amplitude.

(7) Set the channel A level control to the desired trigger level or to PRESET to trigger at ≅(0) zero volts.

(8) Set the AC/DC coupling to AC or DC on channel A.

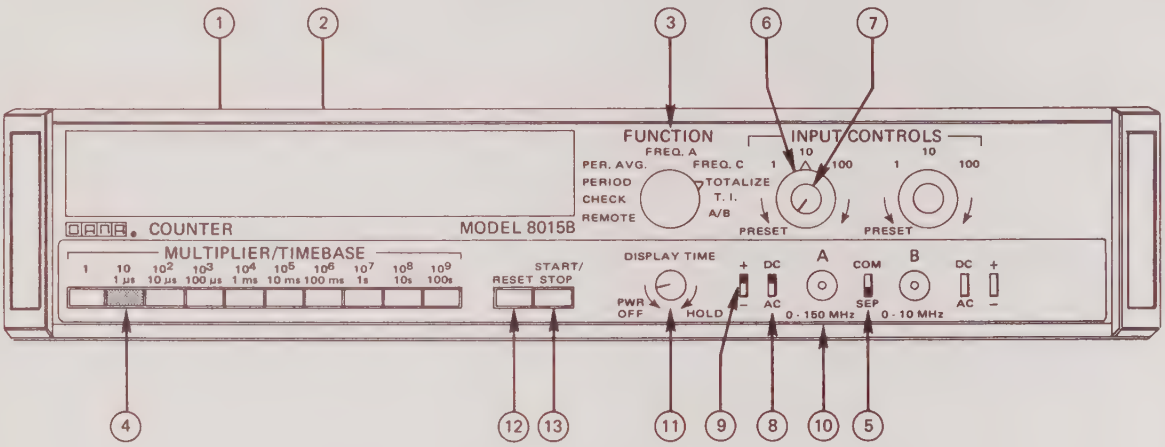
(9) Set the channel A slope to (+) or (–) minus.

(10) Connect the input signal (0 to 10 MHz) to channel A input jack.

(11) Set DISPLAY TIME to a convenient display interval.

Example: Input period to be measured is 1 millisecond at 1V peak. The TIME BASE is set to 1. The channel A input voltage range switch is set to the 1 volt range, the trigger level is set to the PRESET position and AC/DC is set to AC. The display is 0001.0000 milliseconds with 100 nanoseconds resolution. Depress the 10 multiplier switch. The display will be 001.00000 ms with 10 nanosecond resolution.

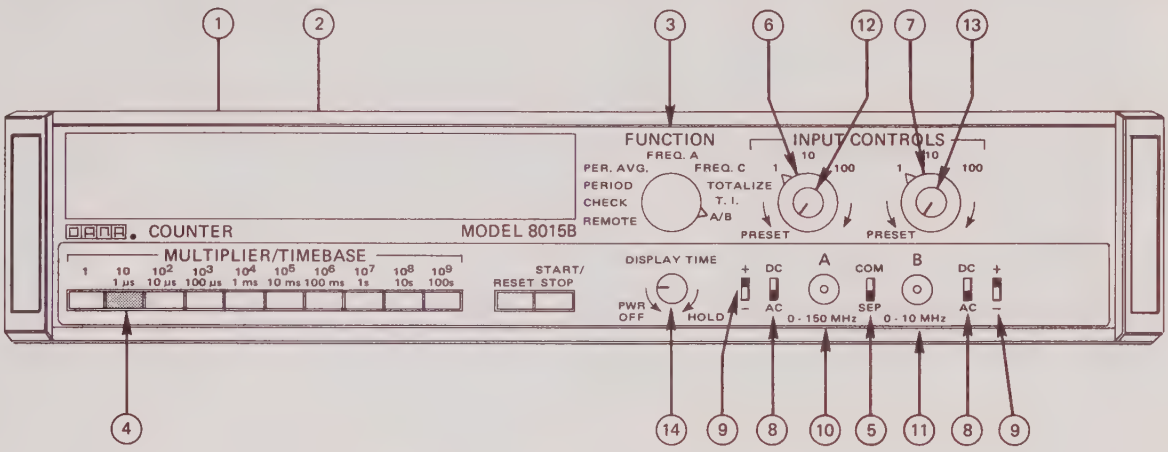
Table 2.6 - Totalize



1. Connect the AC power.
2. Set the STORAGE switch to the ON position. Note: storage automatically disabled.
3. Set the FUNCTION switch to the TOTALIZE position.
4. Set the MULTIPLIER switch for the scaled output desired.
5. Set the SEP/COM switch to the SEP position.
6. Set the channel A INPUT CONTROL range switch to match the input signal amplitude.
7. Set the channel A level control to the desired trigger level or to PRESET to trigger at ≅ (0) zero volts.
8. Set the AC/DC coupling to AC or DC on channel A.
9. Set the channel A slope to (+) plus or (–) minus.
10. Connect the input signal (0 to 150 MHz) to channel A input jack.
11. Turn DISPLAY TIME clockwise to any position. It is not operative in this mode.
12. Depress the RESET switch.
13. To start the count, depress the START/STOP momentary switch. To stop the count, depress the START/STOP switch again.

Example: A series of electrical events is to be counted. They are 10V peak in amplitude and have a rate of 10 kHz. A scaled output is needed at 10 Hz. Set the channel A input voltage range switch to the 10V range, the trigger level to PRESET position, and the AC/DC to AC. The MULTIPLIER switch is set to 10. The count is initiated by depressing the START button. The SCALED OUT will be 10 Hz.

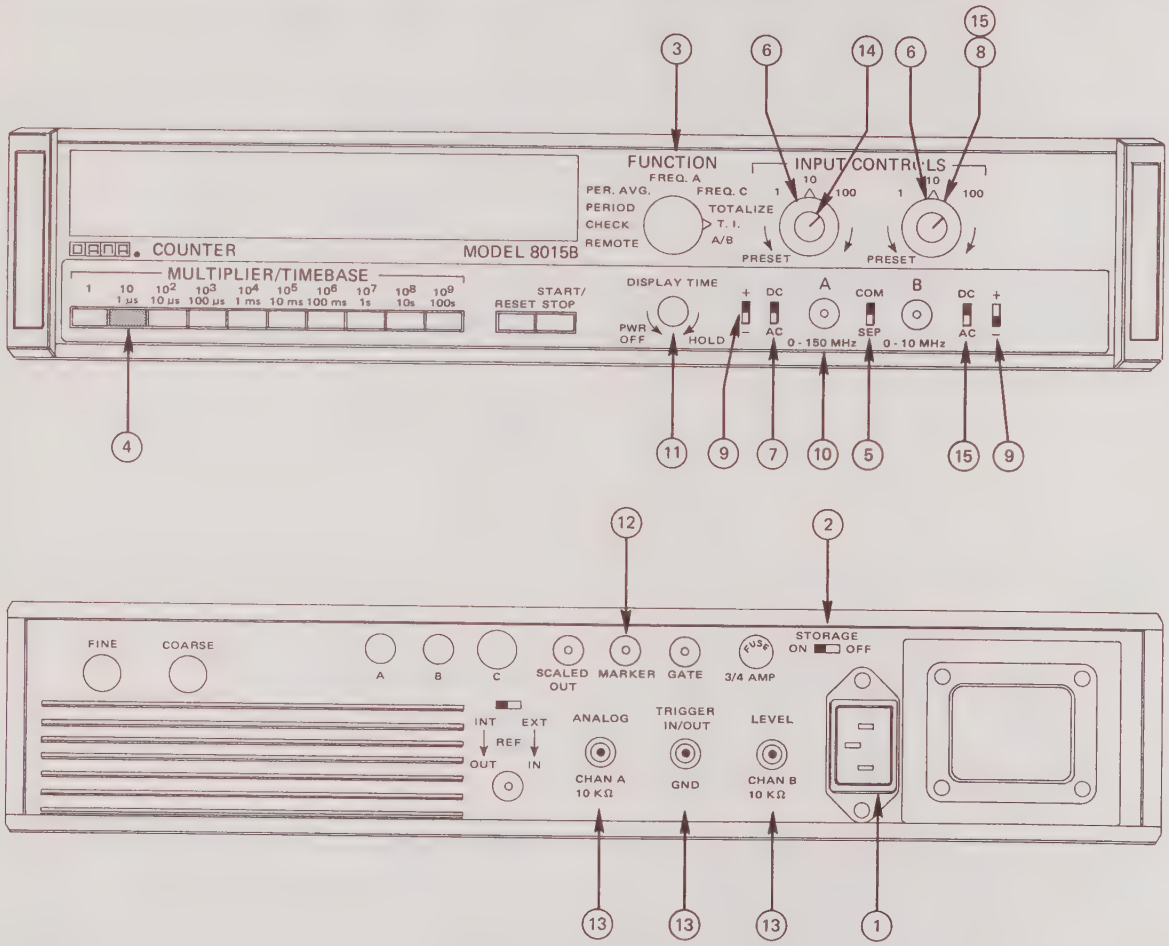
Table 2.7 - A/B Ratio



1. Connect the AC power at the rear panel.
2. Set the STORAGE switch to the ON position.
3. Set the FUNCTION switch to the A/B position.
4. Set the MULTIPLIER switch for the multiplier desired.
5. Set the SEP/COM switch to the SEP position.
6. Set the channel A INPUT CONTROL range switch to match the input signal amplitude.
7. Set the channel B INPUT CONTROL range switch to match the input signal amplitude.
8. Set channel A and B coupling to AC or DC.
9. Set channel A and B slope to (+) plus or (–) minus.
10. Connect the higher frequency input (0 - 150 MHz) to channel A.
11. Connect the lower frequency input (0 - 10 MHz) to channel B.
12. Set the channel A trigger level control to the desired trigger level or to the PRESET to trigger at ≅(0) zero volts.
13. Set the channel B trigger level control to the desired trigger level or to PRESET to trigger at ≃(0) zero volts.
14. Set DISPLAY TIME to a convenient display interval.

Example: The ratio of two frequencies, 100 kHz and 1 kHz, are to be measured. The 100 kHz signal is applied to channel A. The 1 kHz signal is applied to channel B. The 1 MULTIPLIER is depressed. The SEP/COM is set to the SEP position. Both A and B trigger levels are set to PRESET position. The display indicates ratio directly. Ratio equals frequency A divided by frequency B times the multiplier. The display is 00000100. Depress the 10 multiplier. The display is 00001000. Depress the 10^2 multiplier. The display is 00010000.

Table 2.8 - Time Interval



1. Connect the AC power.
2. Set the STORAGE switch to the ON position.
3. Set the FUNCTION switch to the TIME INTERVAL position.
4. Set the TIMEBASE switch to the desired TIME BASE position.
5. Set the SEP/COM switch to the COM position.
6. Set the channel A and B INPUT CONTROL range switch to be compatible with the input signal amplitude.
7. Set channel A AC/DC coupling switch to desired setting.
8. Set channel B AC/DC coupling switch to AC and trigger level to PRESET.
9. Set +/– slope switches to desired setting.
10. Connect input signal (0 to 10 MHz) to channel A input.
11. Set DISPLAY TIME to a convenient display interval.
12. To use the MARKER of the counter, tee-off the input signal of channel A input and connect to vertical input of oscilloscope. Connect MARKER output of counter to Z axis of oscilloscope.

continued

Table 2.8 - Time Interval (continued)

(*13) Connect two DC voltmeters capable of reading ±30 VDC to the ANALOG TRIGGER LEVEL outputs. Use the following formula to determine the trigger level voltage.

$$TL = \frac{VR}{10}$$

Where: TL = trigger level
V = voltmeter reading
R = Input control range

Example: The meter reading is 5 volts on the Input Control range 1.

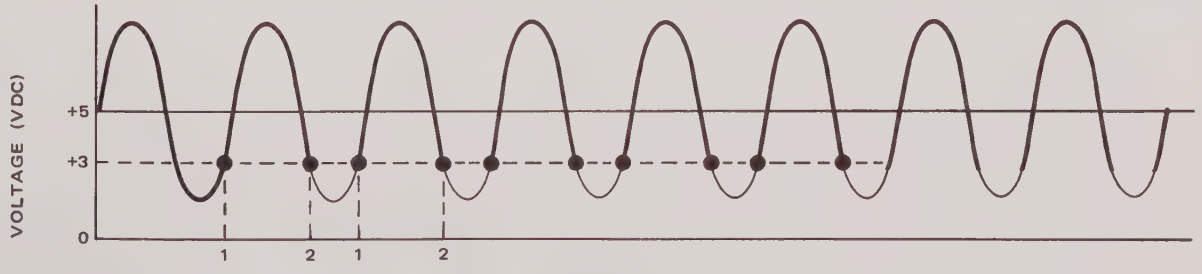
$$TL = \frac{5\,(1)}{10} = .5 \text{ volts}$$

(14) Adjust channel A trigger level control to desired "start" trigger voltage.

(15) Set channel B AC/DC to desired setting and adjust trigger level to desired "stop" trigger voltage.

*Two features are provided in the 8000B counters to aid in setting the front panel controls. These features are the MARKER and the trigger level voltage connectors located on the rear panel. The use of these features is optional.

Example: The input waveform is a 1 kHz 5V peak to peak waveform riding on a 5 volt DC voltage. It is desired to measure the portion of the PERIOD which exist above 3 volts. See figure. Set the TIMEBASE to 1 μsec. Set the SEP/COM to COM. Set the channel A and B input voltage range to 10 volts. Set the A and B coupling to DC. Set the channel A slope to plus and channel B slope to (–) minus. Connect the voltmeters and oscilloscope to the counter as before. Adjust the A trigger level to trigger at 3 VDC on the plus slope. Adjust the B trigger level to trigger at 3 VDC on the minus slope. The period that is measured is intensified on the oscilloscope. The display is 0000746.0 μsec.



1. A TRIGGER LEVEL + SLOPE
2. B TRIGGER LEVEL – SLOPE

SECTION 3 PERFORMANCE CHECK

3.1 INTRODUCTION.

3.2 This procedure is designed to insure that the instrument is operating properly and within its specifications. If any of the readings are not within tolerance, refer to the calibration procedure. If the instrument fails to operate properly, refer to the troubleshooting procedure.

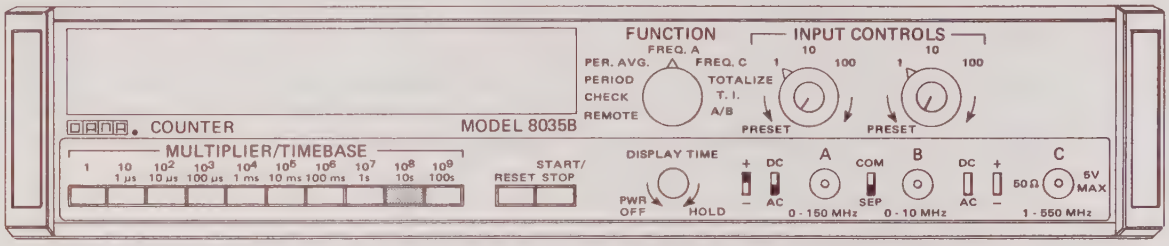
3.3 RECOMMENDED TEST EQUIPMENT.

3.4 Test equipment recommended for the Performance check is listed in table 3.1. Procedures are described in tables 3.2 through 3.11.

Table 3.1 - Required Equipment

Instrument Type	Required Specification	Recommended Instruments
Frequency Standard	5 MHz or 10 MHz	
Oscilloscope	150 MHz Bandwidth	TEK 454
Voltmeter	10 mVDC to 200 VDC	Dana 4300
Sine Wave Generator	2 Hz – 10 MHz	Dana 7010
VHF Signal Generator	10 – 150 MHz	HP8654A
VHF Signal Generator	1 – 550 MHz (Not required for 8010B)	HP8654A
Alignment Tool	.075" Hex (nonmetallic)	General Cement 9300
Alignment Tool	Blade (nonmetallic)	
Sampling Voltmeter	0 – 600 MHz	HP3406
50Ω Feedthru		TEK 011-049
BNC "T" Connectors		
50Ω Tee Connector		HP1022A
2 – BNC to GR Adapters		

Table 3.2 - Reference Oscillator Stability



DISPLAY TIME: Power on/CCW position
FUNCTION Switch: FREQ A
TIME BASE: 10 sec
SLOPE A: (+) Plus
A COUPLING: AC
INPUT VOLTAGE RANGE: 1 Volt
TRIGGER LEVEL A: PRESET
SEP/COM Switch: SEP
STORAGE Switch: ON
REFERENCE Switch: INT

1. Set the controls as shown above.
2. Allow the counter to warmup for 1 hour, except with Option 200, which is 72 hours. Do not remove covers.
3. Connect a 1 MHz at 1V RMS Frequency Standard to Frequency Input A.
4. The difference between the Internal Counter Reference oscillator and the 1 MHz Frequency Standard can be determined by the following formula (20 000 000, – Reading in counts) = the Internal oscillator frequency in hertz.

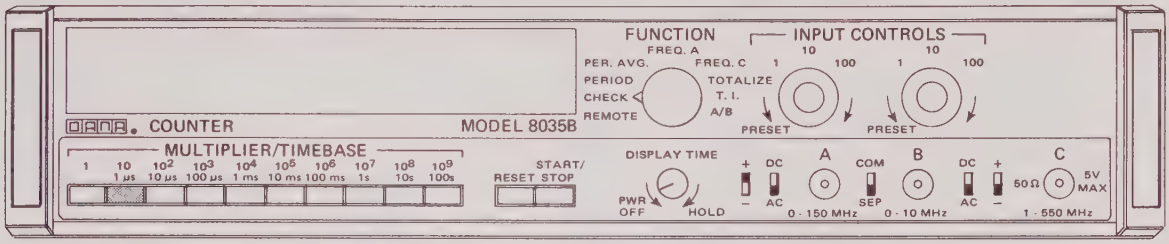
Typical Counter Reference Oscillator Difference for Standard Oscillator

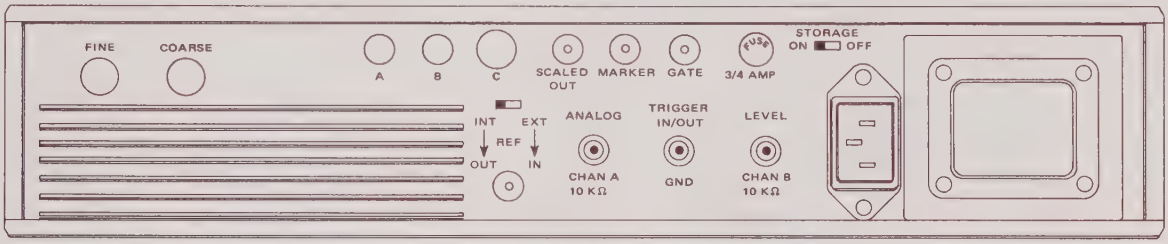
Display	Internal Reference Oscillator
999.9950 kHz	10000.050 kHz
999.9975	10000. 025
1000.0000	10000.000
1000.0025	9999.975
1000.0050	9999.950

5. To calibrate the counter to a Frequency Standard, refer to the Calibration section.
6. To determine long term stability, operate the counter continuously for at least 1 month. The stability is as follows: Standard Oscillator, $< 3 \times 10^{-7}$ per month, Option 050 1×10^{-7} per month, Option 200 1×10^{-9} per day.
7. To measure line voltage stability, use a Variac to vary the line voltage $\pm 10\%$ and measure the frequency difference. The line stability is as follows: Standard Oscillator $\pm 1 \times 10^{-7}$, Option 050 $\pm 5 \times 10^{-8}$, Option 200 $\pm 2 \times 10^{-9}$.
8. To measure temperature stability, vary the temperature from 25°C to 0°. Allow the reading to stabilize and note the reading. Increase the temperature to 50°C and allow the reading to stabilize. The temperature stability 0° to 50°C is as follows: Standard Oscillator $\pm 2.5 \times 10^{-6}$, Option 050 $\pm 5 \times 10^{-7}$, and Option 200 $\pm 5 \times 10^{-9}$.
9. Check the Reference Oscillator output by connecting an oscilloscope to the REF. OUT jack on the rear of the counter. An output of >2.0V peak to peak at 10 MHz is normal.

* No Checked

Table 3.3 - Counting Decades and Multiplier/Timebase Decades





DISPLAY TIME: Power on/CCW position

FUNCTION Switch: CHECK

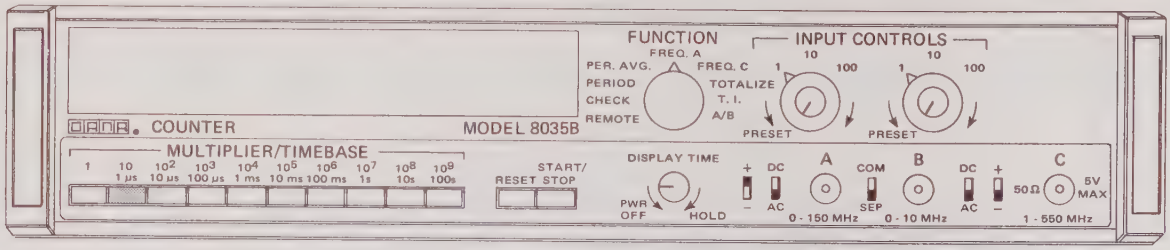
TIME BASE: See chart

STORAGE Switch: ON

REFERENCE Switch: INT

Timebase	Display	Tolerance
1 μs	0 0 0 0 0 0 0 1 0	± 1 count
10	0 0 0 0 0 0 1 0 0	± 1 count
100	0 0 0 0 0 1 0 0 0	± 1 count
1 ms	0 0 0 0 1 0 0 0 0	± 1 count
10	0 0 0 1 0 0 0 0 0	± 1 count
100	0 0 1 0 0 0 0 0 0	± 1 count
1 sec	0 1 0 0 0 0 0 0 0	± 1 count
10	1 0 0 0 0 0 0 0 0	± 1 count
100	0 0 0 0 0 0 0 0 0	± 1 count
9th digit option		

Table 3.4 - Decimal Point and Units



DISPLAY TIME: Power on/CCW position

FUNCTION Switch: Set for each check

TIME BASE: See table below

STORAGE Switch: ON

REFERENCE Switch: INT

Timebase	DISPLAY			
	FREQ A	Units	FREQ C (Not in 8015B)	Units
1 µsec	000000000	MHz	000000000	MHz
10	00000000.0	MHz	00000000.0	MHz
100	0000000.00	MHz	0000000.00	MHz
1 ms	000000.000	MHz	000000.000	MHz
10	00000.0000	MHz	00000.0000	MHz
100	0000.00000	MHz	0000.00000	MHz
1s	000.000000	MHz	000.000000	MHz
10	00000.0000	kHz	00.0000000	MHz
100	0000.00000	kHz	0.00000000	MHz
9th digit option				

PERIOD

Multiplier Selected	Display	Units
1	00000000.0	µsec
10	000000000	µsec
10^2	0000000.00	msec
10^3	00000000.0	msec
10^4	000000000	msec
10^5	0000000.00	sec
10^6	00000000.0	sec
10^7	000000000	sec
10^8	000000000	–
10^9	000000000	–
9th digit option		

continued

Table 3.4 - Decimal Point and Units (continued)

PERIOD AVERAGE

Multiplier Selected	Display	Units
1	00000.0000	msec
10	0000.00000	msec
10^2	000.000000	msec
10^3	00000.0000	μsec
10^4	0000.00000	μsec
10^5	000.000000	μsec
10^6	00000.0000	nsec
10^7	0000.00000	nsec
10^8	000.000000	nsec
10^9	000000000	–
9th digit option ⟶		

TIME INTERVAL

Multiplier Selected	Display	Units
1	0000000.00	μsec
10	00000000.0	μsec
10^2	000000000	μsec
10^3	0000000.00	msec
10^4	00000000.0	msec
10^5	000000000	msec
10^6	0000000.00	sec
10^7	00000000.0	sec
10^8	000000000	sec
10^9	000000000	–
9th digit option ⟶		

TOTALIZE
A/B RATIO

Verify that no annunciators except the gate are lit when any multiplier button is depressed.

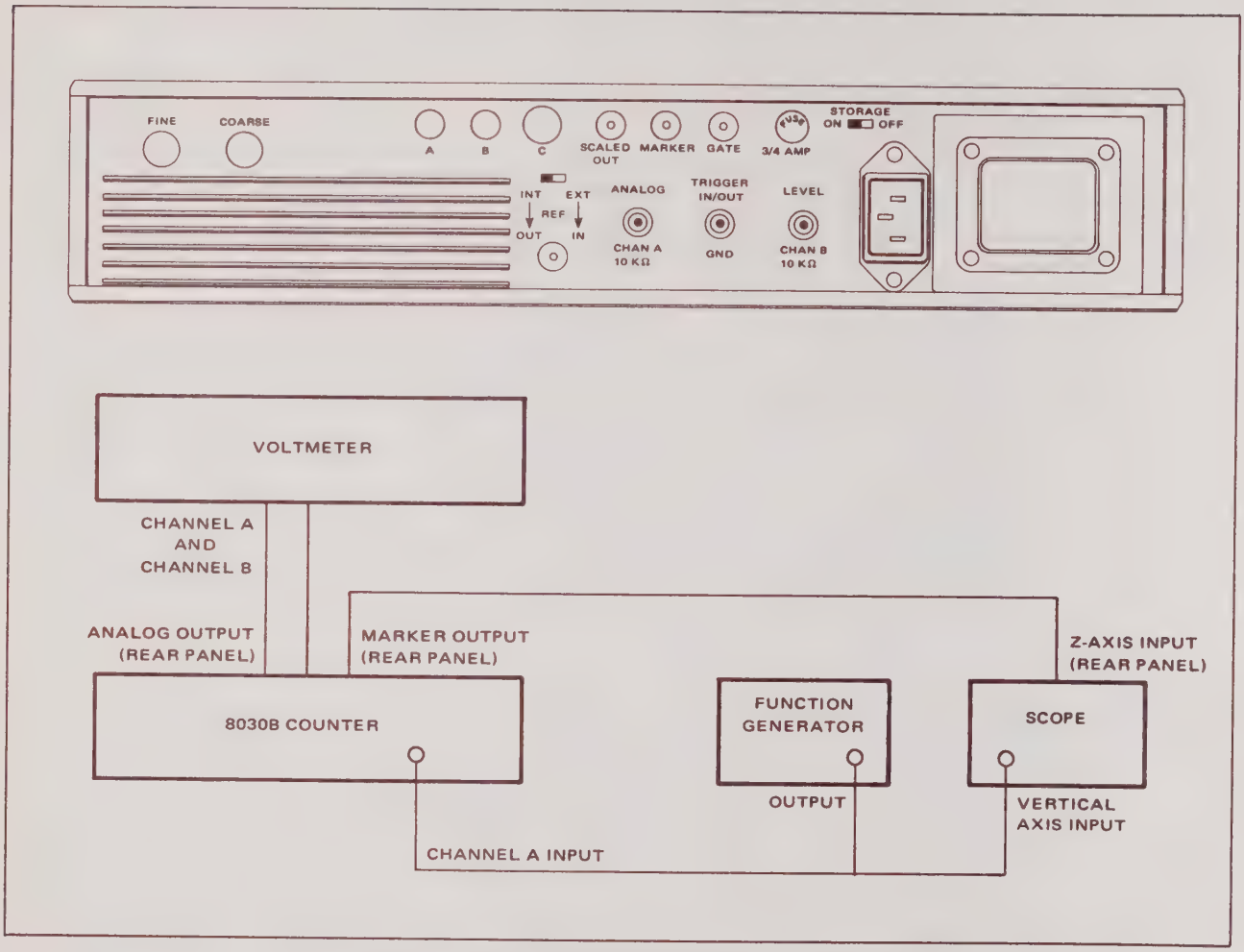
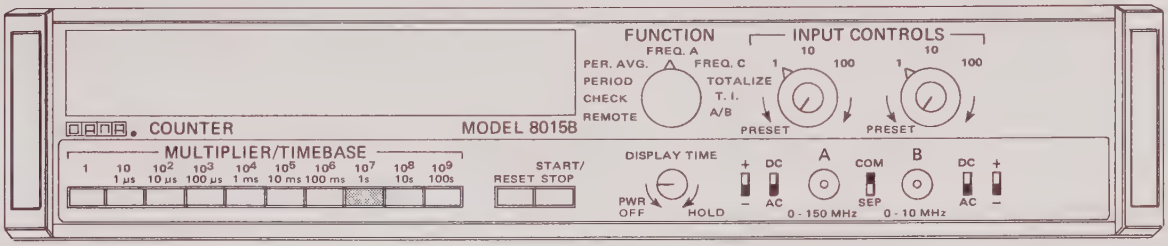


Figure 3.1 - Input Control and Marker Check Connections

Table 3.5 - Input Controls and Marker



DISPLAY TIME: Power on/CCW position
FUNCTION: FREQ A
TIME BASE: 1 second
SLOPE A: Minus (–)
SLOPE B: Minus (–)
COUPLING A: AC
STORAGE: ON (rear panel)

COUPLING B: AC
INPUT RANGE CONTROL A: 1
INPUT RANGE CONTROL B: 1
TRIGGER LEVEL A: PRESET
TRIGGER LEVEL B: PRESET
SEP/COM: COM

1. Set counter controls as shown above.

2. Connect Function Generator output to Input A on the counter. Also connect the Function Generator to the vertical input on an oscilloscope. Refer to figure 3.1 for all connections.

3. Adjust the Function Generator to 100 Hz at 4V peak to peak sine wave. Adjust the oscilloscope for a trace.

4. Connect voltmeter to the channel A Analog Output on the rear panel of the counter. For counters with Option 008, Systems Interface, connect to J110-S and J110-15.

5. Verify that the marker initiation is ±50 mVDC on the negative slope. Vary the channel A trigger level control and verify the marker initiation is variable over +3 volts to –3 volts on the negative slope of the sine wave.

6. Return channel A trigger level to the Preset position. Change channel A slope to (+) plus. Verify that the marker initiation is ±50 mVDC on the positive slope. Vary channel A trigger level control and verify the marker initiation is variable over +3 volts to –3 volts on the positive slope of the sine wave on the oscilloscope.

7. Return the channel A trigger level to Preset and the channel A slope to (–) minus.

8. Connect a voltmeter to the channel B Analog Output on the rear panel of the counter. For counters with Systems Interface, connect to J110-N and J110-15.

9. Verify that the marker termination is ±50 mVDC on the negative slope. Vary the channel B trigger level control and verify that the marker termination is variable over +3 volts to –3 volts on the negative slope of the sine wave.

10. Return channel B trigger level to Preset position. Change channel B slope to (+) plus. Verify that the marker termination is ±50 mVDC on the positive slope. Vary channel B trigger level control and verify the marker initiation is variable over +3 volts to –3 volts on the positive slope of the sine wave on the oscilloscope.

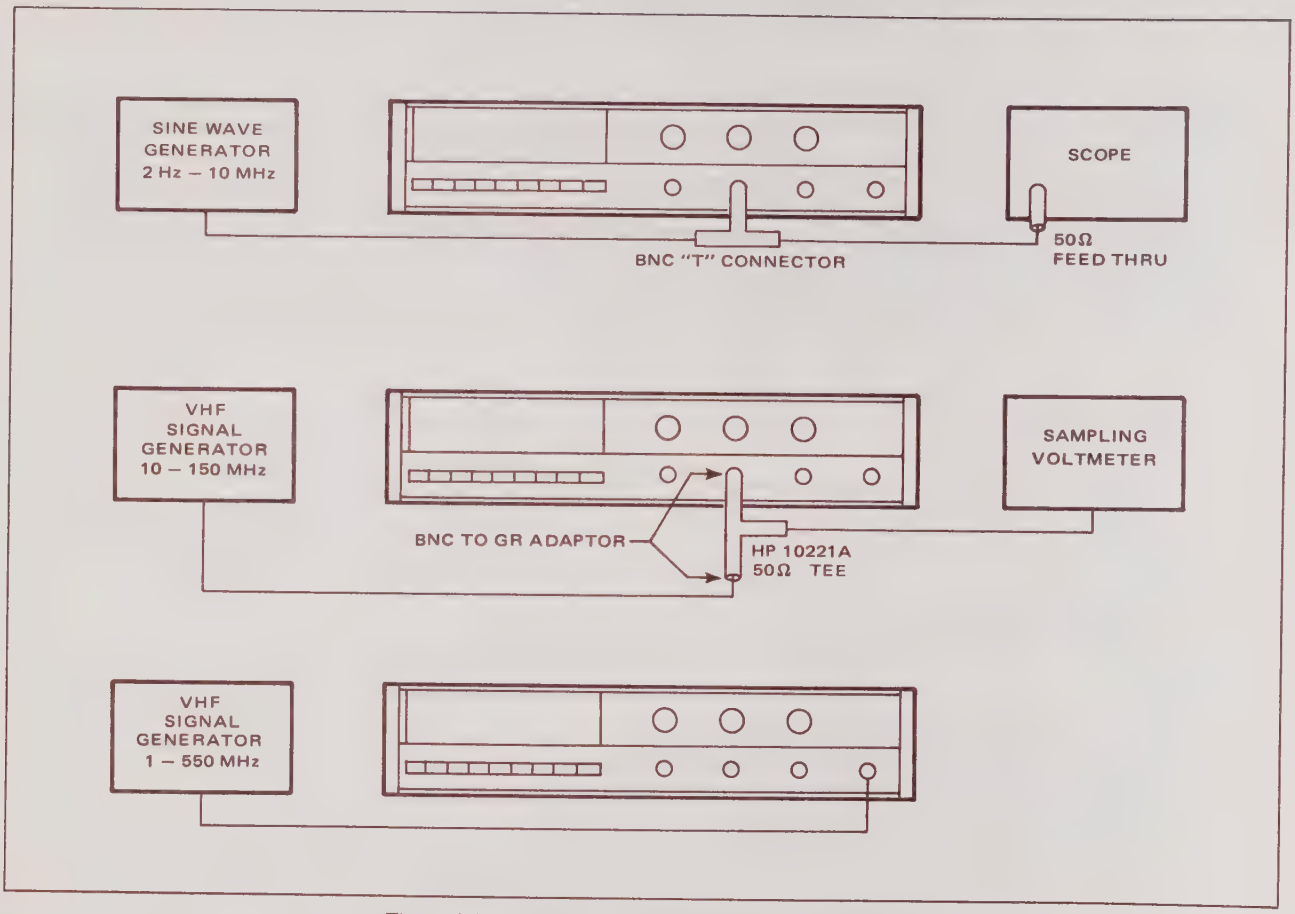
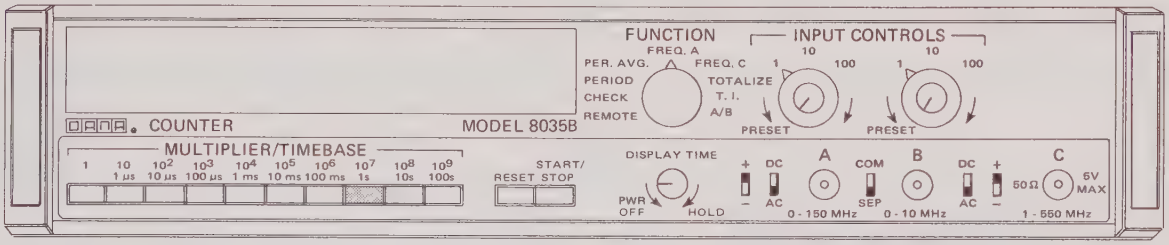


Figure 3.2 - Frequency Response Check Connections

Table 3.6 - Frequency Response and Sensitivity



DISPLAY TIME: Power on/CCW position
FUNCTION: FREQ A
TIME BASE: 1 second
SLOPE A: (+) Plus
SLOPE B: (+) Plus
COUPLING A: AC
STORAGE: ON

COUPLING B: AC
INPUT RANGE CONTROL A: 1
TRIGGER LEVEL CONTROL A: PRESET
INPUT RANGE CONTROL B: 1
TRIGGER LEVEL CONTROL B: PRESET
SEP/COM: SEP

1. Set controls as shown above.

2. Connect a BNC "T" connector to channel A input. Connect a sine wave generator (2 Hz – 10 MHz) and an oscilloscope to the "T" connector. Use a 50 ohm termination at the vertical input to the oscilloscope. Refer to figure 3.2 for hookup.

3. Adjust the sine wave generator between 10 Hz to 10 MHz maintaining 50 mV RMS output. Verify that the counter displays the frequency through this range. Change the A slope to (–) minus. Verify that the counter displays the frequency through this range.

4. Replace the sine wave generator with a VHF signal generator. Connect generator as shown in figure 3.2 and adjust for a 50 mV RMS output.

5. Set the Time Base to 1 second and the A slope to (+) plus.

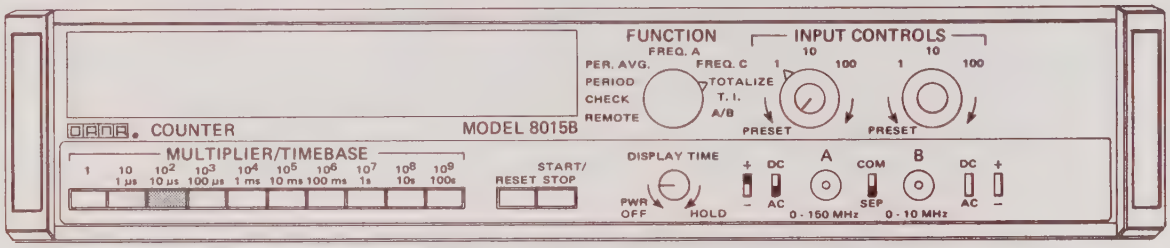
6. Vary the signal generator from 10 MHz to 100 MHz. Verify that the counter displays the frequency.

7. Set the output of the VHF signal generator to 100 mV RMS. Vary the signal generator from 100 MHz to 150 MHz. Verify that the counter displays the frequency.

8. Frequency C Model 8035B. Change the function to Frequency C. Connect the VHF signal generator as shown in figure 3.2 and set the output to 50 mV RMS (for Option 030, set the output to 1 mV RMS). Vary the VHF signal generator between 1 MHz and 550 MHz (for Option 030, 10 MHz to 500 MHz).

9. The counter should display all frequencies in this range.

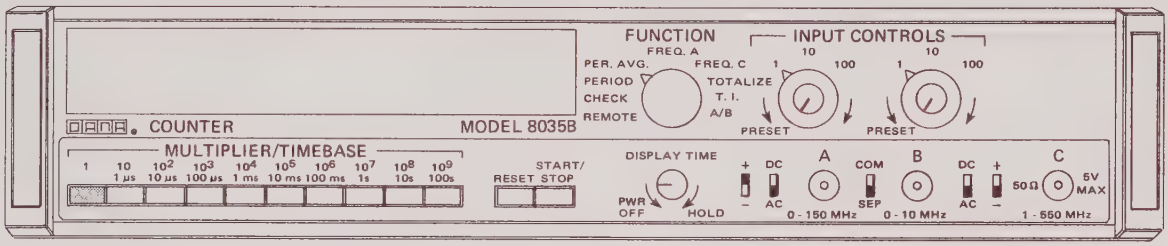
Table 3.7 - Totalize



DISPLAY TIME: Power on/CCW
FUNCTION: TOTALIZE
MULTIPLIER: 10^3
INPUT VOLTAGE RANGE A: 1
TRIGGER LEVEL A: PRESET

1. Set the counter controls as shown above.
2. Connect test oscillator to the counter at Input A. Set the oscillator output to .5V RMS at a frequency of 1 MHz.
3. Connect an oscilloscope to the scaled output jack on the counter rear panel.
4. Push the Reset on the counter. The display should read all zeros. Push the Start/Stop button. The display should totalize.
5. The scaled out should be a series of pulses with an amplitude of greater than 2V P.P. The scaled out repetition rate will be 10 kHz.
6. Depress the Start/Stop again. Totalizing should stop and the accumulated count should be displayed.
7. Push the Reset button and the display should be all zeros.

Table 3.8 - Period and Period Average



DISPLAY TIME: Power on/CCW
FUNCTION: PERIOD
MULTIPLIER: 1

INPUT VOLTAGE RANGE: 1
INPUT TRIGGER LEVEL A: PRESET

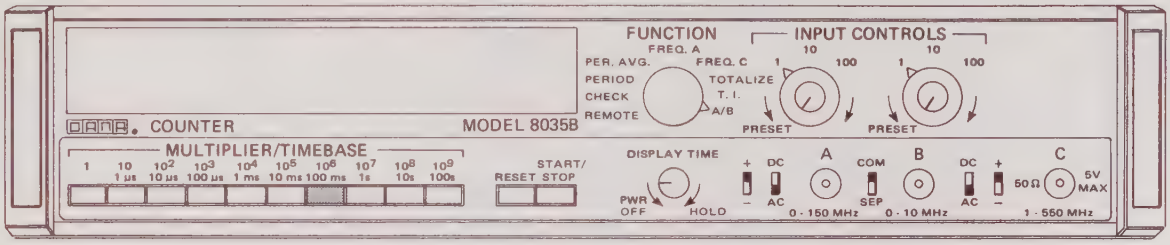
PERIOD

1. Set the counter controls as shown above.
2. Connect a test oscillator to Input A. Adjust the output of the oscillator to .5V RMS.
3. Vary the test oscillator frequency between 10 Hz and 10 MHz. The counter will display the period of the frequency.

PERIOD AVERAGE.

1. Set the Function switch to Period Average. Set the multiplier to 10.
2. Vary the test oscillator frequency between 10 Hz and 10 MHz.
3. The counter will display the period by taking the average period of the periods averaged.

Table 3.9 - A/B Ratio

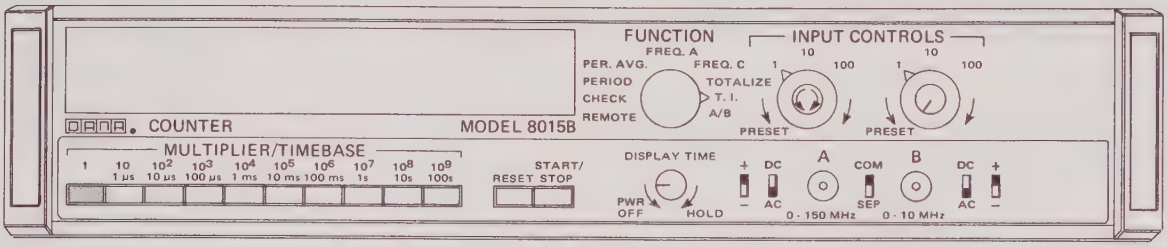


DISPLAY TIME: Power on/CCW
FUNCTION: A/B
MULTIPLIER: 10^6
SLOPE (A and B): (+) Plus
COUPLING (A and B): AC
INPUT VOLTAGE RANGE (A and B): 1
SEP/COM: COM
STORAGE: ON
TRIGGER LEVEL (A and B): PRESET

A/B RATIO

1. Set controls as shown above.
2. Adjust test oscillator output to 10 MHz at 100 mV RMS.
3. Connect test oscillator to Input A.
4. Counter should display 1000000 counts.

Table 3.10 - Time Interval



DISPLAY TIME: Power on/CCW
FUNCTION: T. I.
MULTIPLIER: 1
SLOPE A: (+) Plus
SLOPE B: (+) Plus
COUPLING A: AC
COUPLING B: AC

INPUT VOLTAGE RANGE A: 1
INPUT VOLTAGE RANGE B: 1
SEP/COM: COM
STORAGE: ON
TRIGGER LEVEL A: Adjust
TRIGGER LEVEL B: PRESET

TIME INTERVAL

1. Set controls as shown above.

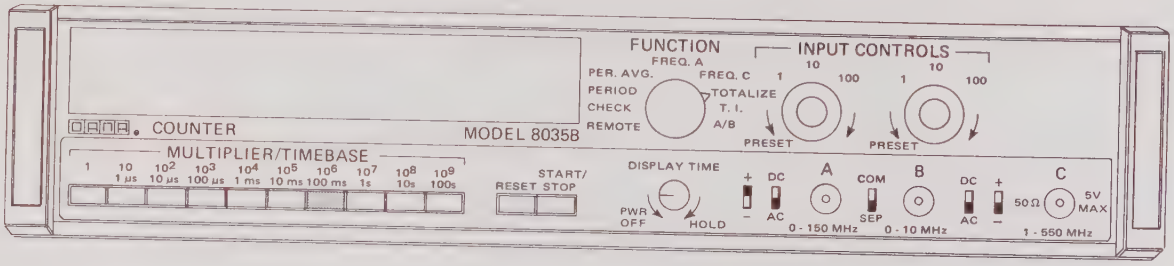
2. Connect pulse generator output and oscilloscope to a "T" connector. Connect the "T" connector to the input "A" on the counter. Use a 50 ohm feed through on the input to the oscilloscope.

3. Adjust the pulse generator output to 900 kHz repetition rate, with a 200 nanosecond pulse width at 1V peak to peak.

4. The counter will display the period of the waveform.

5. Set slope B to (–) minus. The counter will display pulse width.

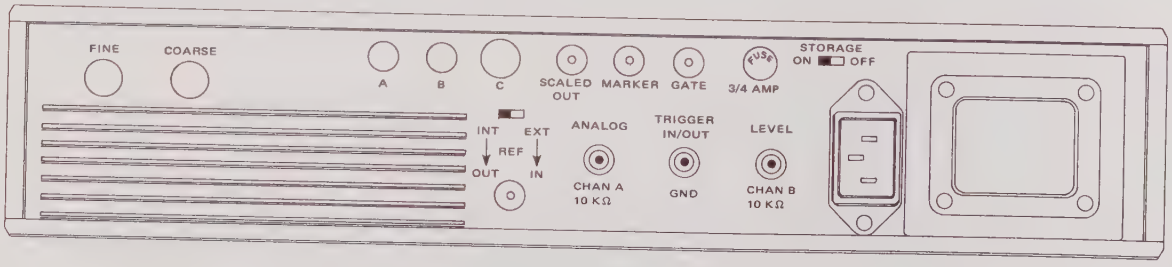
Table 3.11 - Display Time and Gate Output



DISPLAY: Power on/CCW

FUNCTION: TOTALIZE

1. Set controls as shown above.
2. Connect the vertical input of an oscilloscope to the gate output on the counter rear panel.
3. Press Reset and check that the gate output is low.
4. Press Start/Stop and check that the gate output is greater than 2V.
5. Press Start/Stop again and check that the gate output is low.
6. Set the Function switch to Frequency A and the Time Base to 100 msec.
7. Vary the Display Time and check that the repetition rate changes from approximately 30 milliseconds to 5 seconds.



SECTION 4 THEORY OF OPERATION

4.1 GENERAL.

4.2 This section covers the theory of operation of the Series 8000B Counter. Operation of the unit is dependent on the measurement mode selected. For this reason, general operating principles of each mode of operation are described first followed by individual circuit descriptions. Where circuitry differences occur between models, the models covered are identified.

4.3 Drawings in this section are included for explanation only. For specific reference designators, wiring details, etc., refer to the complete schematics in Section 6.

4.4 MEASUREMENT MODES.

4.5 Figures 4.2 through 4.10 summarize the basic principles of each operating mode in simplified form. Any point (positive or negative) on the input waveform can be selected to trigger the generation of pulses to the main gate.

4.6 The block labeled "counter" refers to both a high-speed decade on the Switch board and the display counter. The high-speed decade divides its input by 10 and advances the display counter. It also updates the least-significant readout position (figure 4.1).

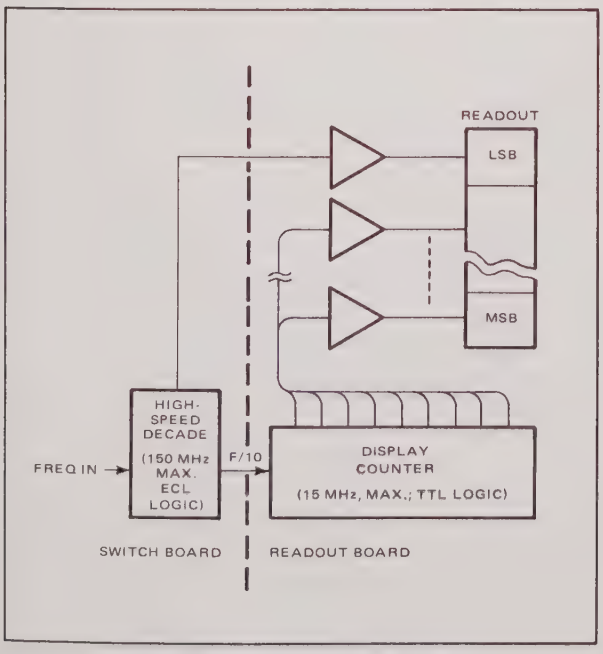


Figure 4.1 - Counter Definition

4.7 The "Display" block includes quad-latches and drivers for each of the readout positions (bits), and the readout tubes.

4.8 The "Reference Frequency" block can be either an external reference frequency or the internally generated reference frequency. The internal reference includes the reference oscillator (on Readout board), and the reference conditioning circuits (on the Switch board).

4.9 "Main Gate" refers to the logic that generates the signal $\overline{\Delta t}$. This signal controls the times at which the counter begins or stops counting. Counter operation is dependent on the mode of operation and other selections made by the operation (timebase, input trigger level, etc).

4.10 Self-Check Mode.

4.11 The Self-Check mode of operation (figure 4.2) enables the operator to check for proper operation of the counter. The reference frequency is used for two purposes. It is counted by the counter during the measurement time and it generates the time base frequency that produces the gating signal. Proper operation of the counter is determined by varying the time base and observing the readout (see Section 3, table 3.3).

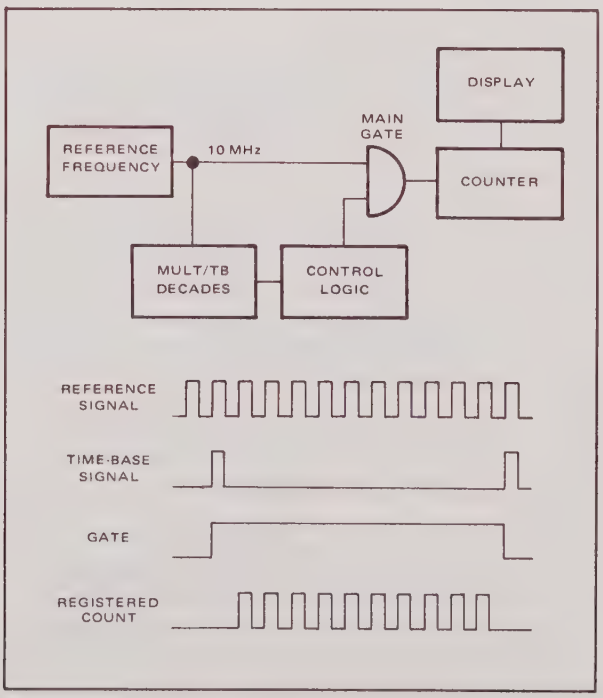


Figure 4.2 - Self-Check Mode

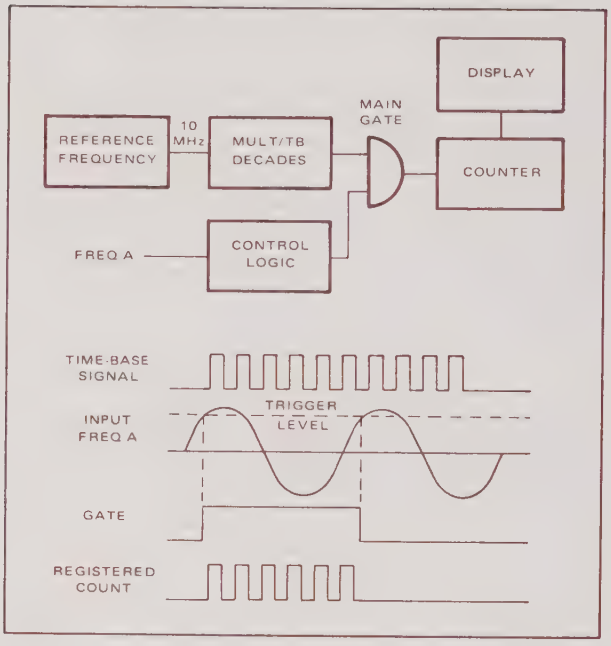


Figure 4.3 - Period Mode

4.12 Period Mode.

4.13 Period is the inverse of frequency. Therefore, frequency A is applied to the control logic and the reference frequency is connected to the multiplier/timebase decades (figure 4.3).

4.14 Clock pulses are derived by dividing down the 10 MHz reference oscillator output. The specific decade division is determined by the setting of the MULTIPLIER/ TIMEBASE switches. The output of the M/TB decades is presented to the input of the counter. Trigger pulses resulting from two consecutive signals from input A are applied to the control logic. The first trigger pulse opens the main gate; the next pulse closes it. During "gate open" time, the counter counts the applied clock pulses. The count is displayed on the readout directly in microseconds, milliseconds, or seconds, according to the MULTIPLIER/ TIMEBASE switch setting.

NOTE

Low Frequencies may be determined more accurately by measuring period rather than frequency directly. This is because the longer period of a low frequency allows more counts to accumulate in a period measurement. Therefore, resolution and accuracy are both improved.

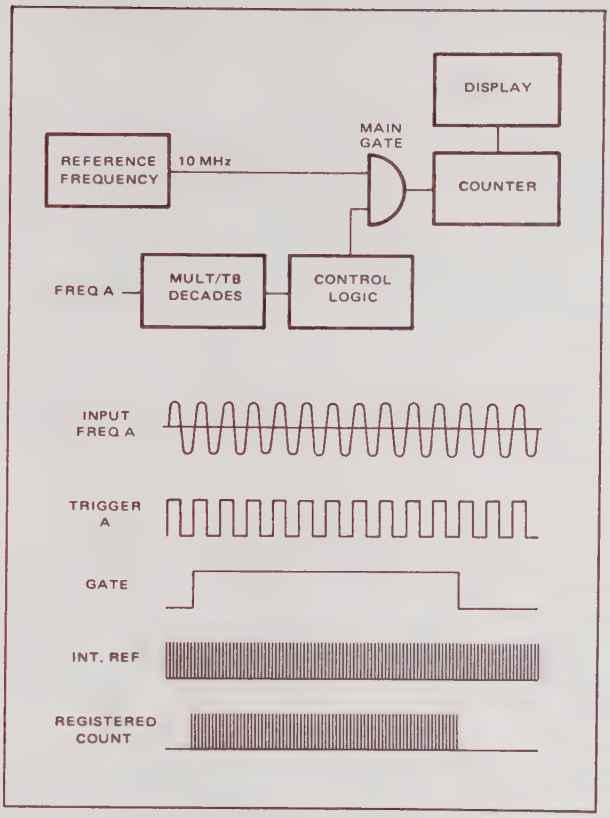


Figure 4.4 - Period Average Mode

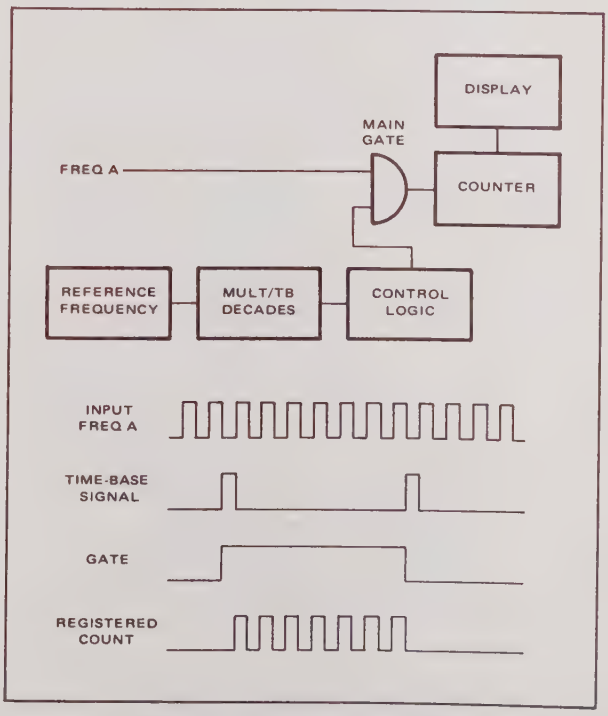


Figure 4.5 - Frequency "A" Mode

4.15 Period Average Mode.

4.16 Period Average mode is used to obtain increased resolution and accuracy over period measurements. The more periods over which a signal is averaged, the greater the accuracy of the measurement.

4.17 In this mode of operation (figure 4.4), the reference oscillator is routed directly to the main gate and the unknown frequency is routed through the multiplier/time base decades to the control logic which, in turn, controls the main gate. The pulses occurring during main "gate open" are counted, stored, and an accurate readout measurement is displayed. The "gate open" period is determined by the setting of the MULTIPLIER/TIMEBASE switches.

4.18 Frequency A Mode.

4.19 During direct frequency measurements, the counter compares the unknown frequency against the known reference frequency (figure 4.5).

4.20 Input signal F_a is routed to the main gate of the counter. The internal reference supplies a 10 MHz signal through the multiplier/time base decades and through the control logic to control the main gate.

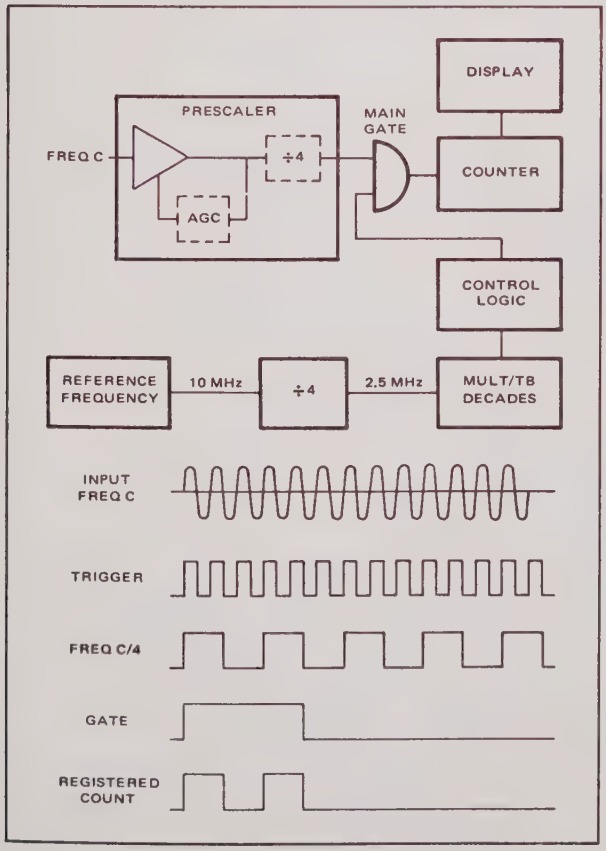


Figure 4.6 - Frequency C Mode

4.21 The number of input pulses accumulated during the main "gate open" interval is a measurement of the input frequency. The count obtained is displayed on the readout. This display may be retained until such a time as a new sample is ready to be displayed.

4.22 Frequency C Mode. (Not available in Model 8015B.)

4.23 In the Frequency C mode, the unknown frequency is applied to the main gate through the prescaler. The prescaler includes an amplifier, automatic gain control circuit, and a divide-by-four circuit (figure 4.6).

4.24 The AGC circuit maintains the required amplifier gain which alleviates the need for manual trigger and range control. The divide-by-four circuit is necessary to reduce the unknown frequency to a frequency which the main counter circuitry can count. The reference frequency is also divided by four to enable direct readout. The actual gate time is four times the selected time base.

4.25 Totalize Mode.

4.26 In Totalize mode, the main gate is controlled by the manual START/STOP switch on the front panel of the instrument or external START/STOP commands (figure 4.7).

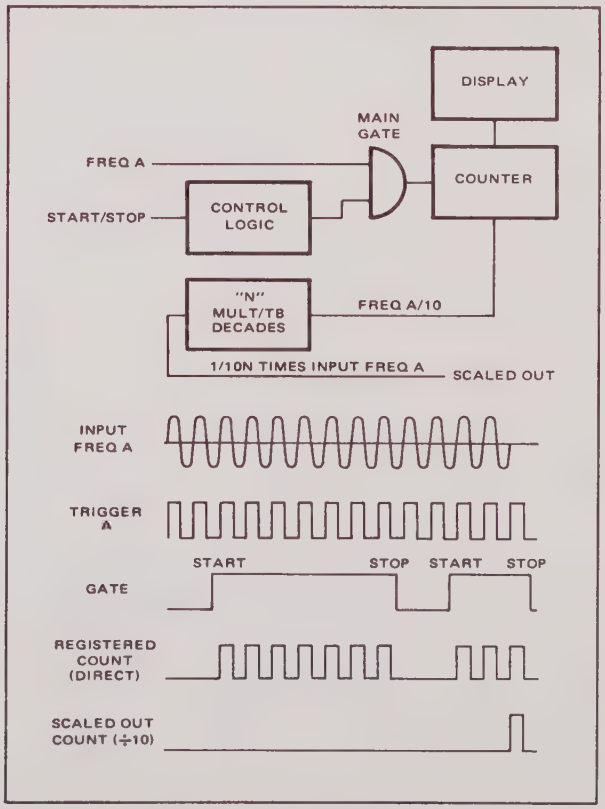


Figure 4.7 - Totalize Mode

4.27 With the first Start/Stop command, the control logic opens the main gate allowing the input pulses to be totalized by the counter. Simultaneously, a continuous update is supplied to the flip-flops which make up the display latches. The counter readout then represents the input pulses received during the interval between "start" and "stop". External start/stop commands may be applied via the REMOTE connector if equipped with the systems interface option.

4.28 In this mode, the instrument delivers a scaled output frequency to a connector on the rear panel, SCALED OUT. The output is the input signal frequency scaled by 1/10N where N is the multiplier setting.

4.29 Time Interval Mode (Figures 4.8 and 4.9).

4.30 The Time Interval mode of operation allows measurement of the time between two electrical events. The first event (start) is connected to channel A input and opens the gate. The second event (stop) is connected to the channel B input and closes the gate. The internal reference supplies a frequency of 10 MHz to a X10 multiplier (harmonic generator) (figure 4.8). The resulting 100 MHz frequency is applied to the gate. With a timebase of 1, the counter advances at a 100 MHz rate providing a resolution of 10 nanoseconds. With a timebase of 10, the counter advances at a rate of 10 MHz providing a resolution of 100 nanoseconds (figure 4.9). Increasing timebase selections step down the counting rate accordingly. Slope and trigger level controls on the front panel allow a variable trigger level on the plus or minus slope of the input waveforms. The resolution is 10 nsec and the range is 10^8 or 10^9 with Option 004, 9th digit. Channel A can be triggered after channel B trigger in 30 ms on a single time interval measurement.

4.31 The pulses occurring during the main gate are counted and displayed. Channel A can be triggered after the channel B trigger in 30 ms on a single time interval measurement.

4.32 A/B (Ratio) Mode.

4.33 This mode is identical in function to the frequency measurement modes, but substitutes an external signal for the reference frequency (figure 4.10).

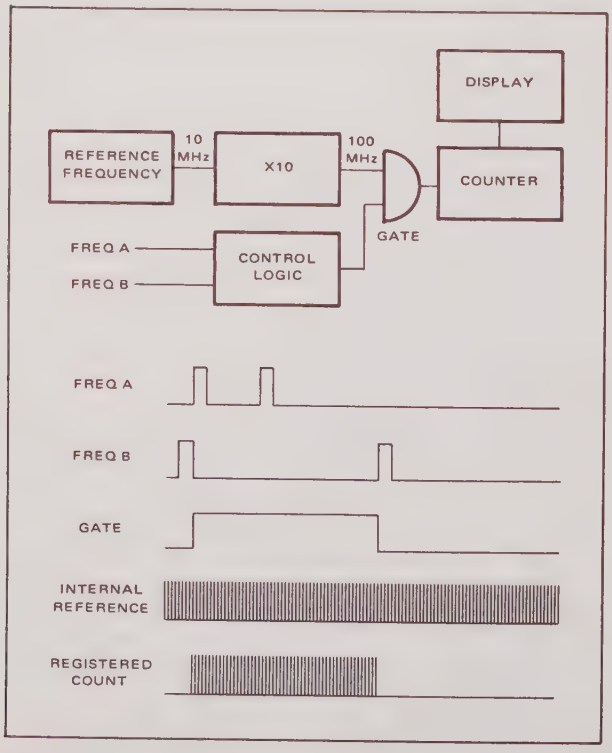


Figure 4.8 - Time Interval Mode (10 ns Resolution)

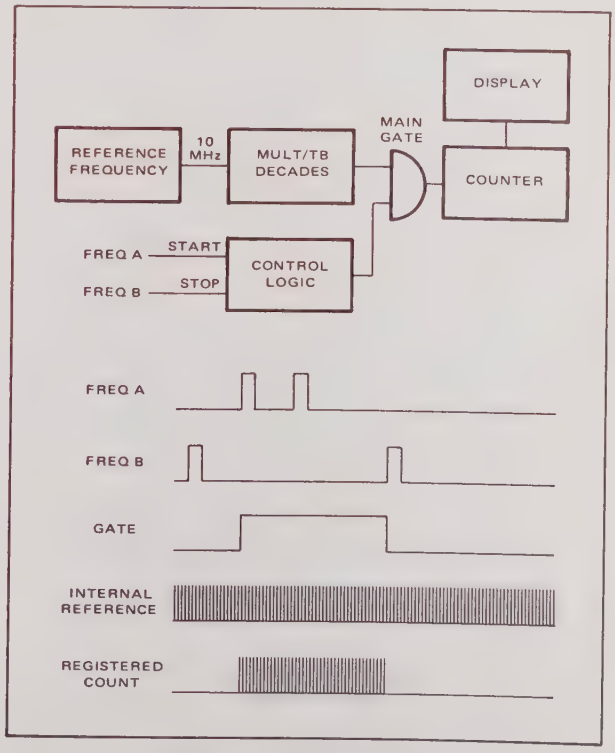


Figure 4.9 - Time Interval Mode

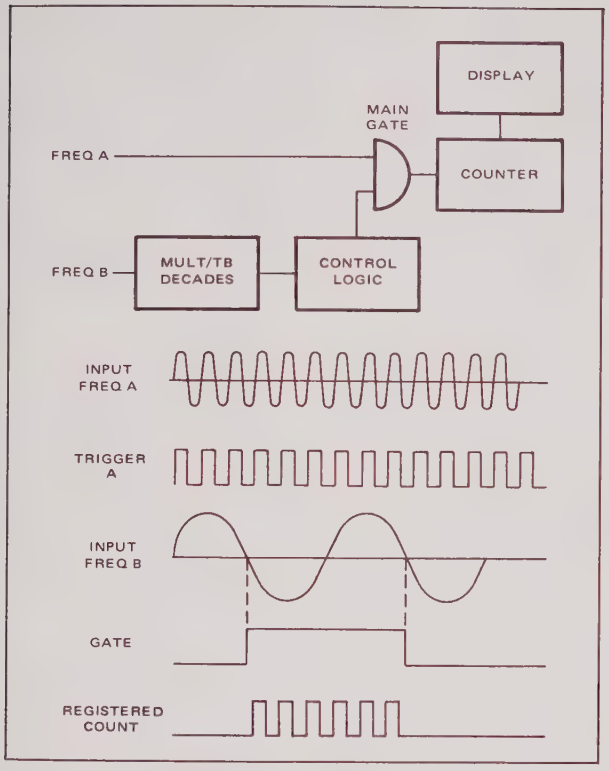


Figure 4.10 - A/B Ratio Mode

4.34 The higher of the two frequencies which are to be measured is connected to input A; the lower frequency to input B. Input B is applied to the multiplier/timebase decades. The higher the multiplier/timebase selected, the greater the resolution and the longer the measurement time. Two successive trigger pulses derived from the multiplier/timebase decades applied to input B open and close the main gate. During the "gate open" interval, the counter counts the trigger pulses derived from input A and the ratio Fa/Fb is then displayed on the readout.

4.35 CIRCUIT DESCRIPTIONS.

4.36 A block diagram of the counter is shown in figure 4.11. The circuit descriptions to follow make reference to the schematics in Section 6 as well as to partial schematics within this section.

4.37 Prescaler (Schematic: figures 6.13 and 6.15). Not available in Model 8015B.

4.38 The Prescaler provides the signal conditioning function for channel C. It accepts frequencies from 1 MHz to 550 MHz (10 MHz to 500 MHz with 030 option), automatically controls the amplitude of the signal, and divides the frequency of the signal by a factor of four. The scaling reduces the incoming signal to a rate compatible with the

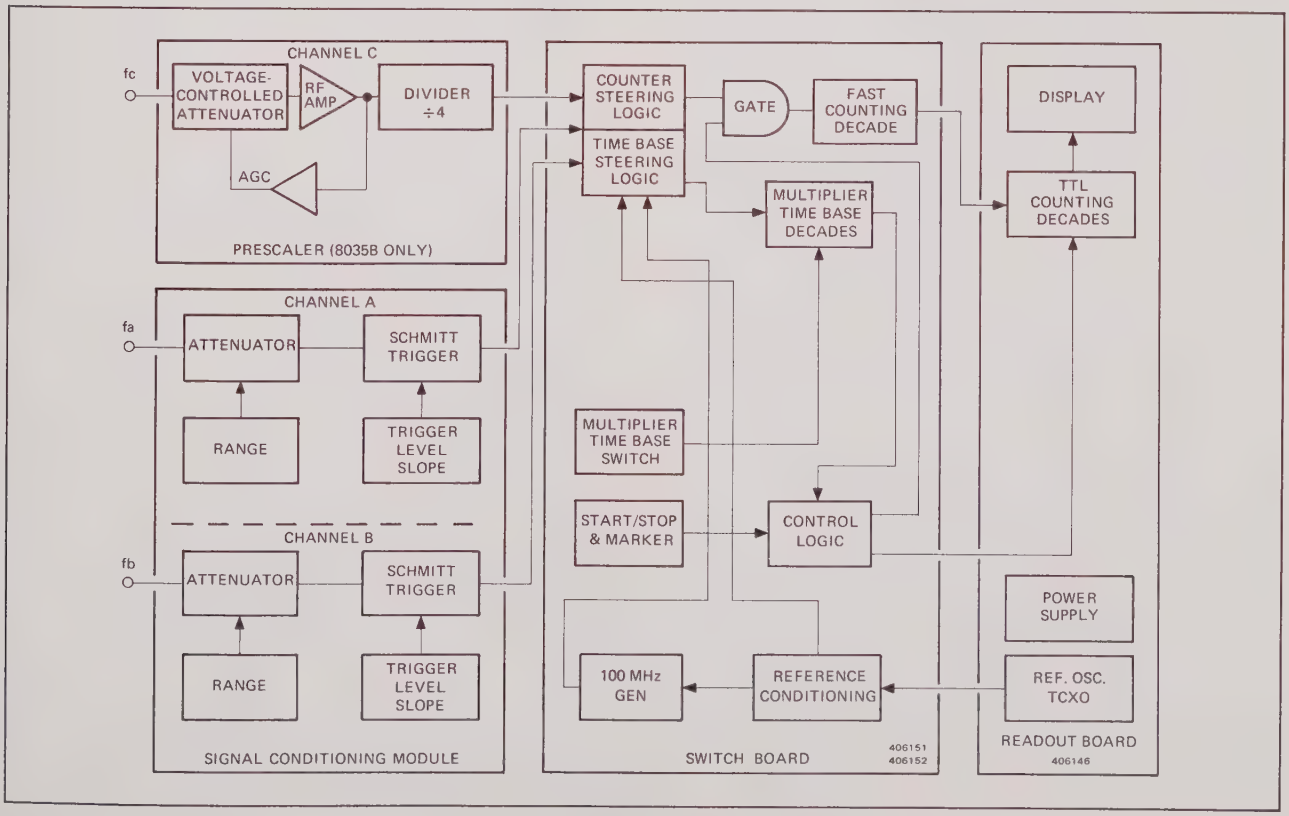


Figure 4.11 - Functional Block Diagram

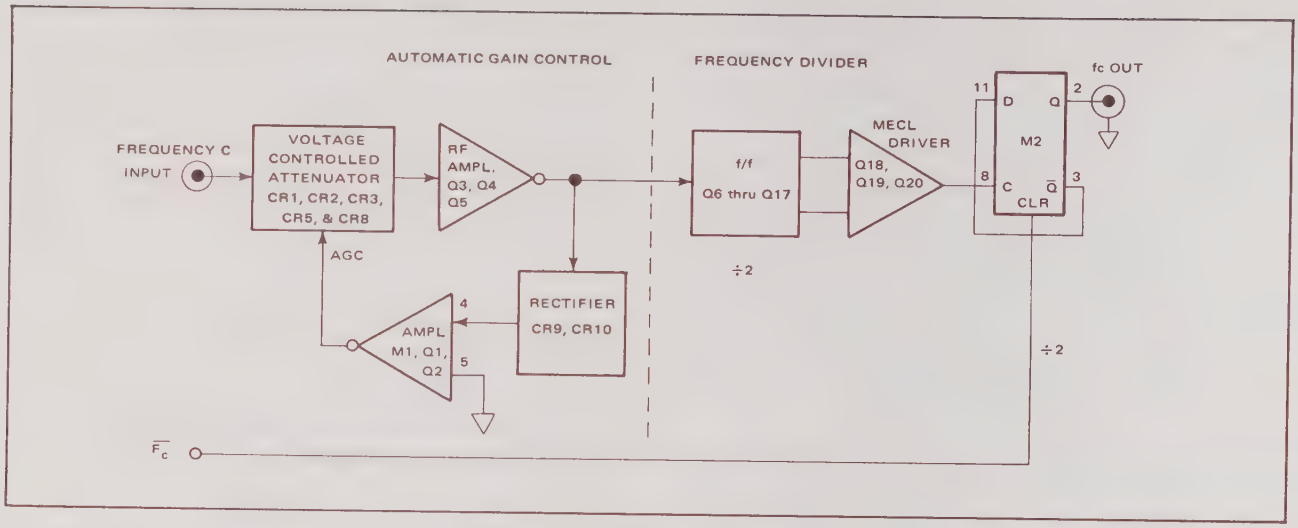


Figure 4.12 - 550 MHz Prescaler

high-speed decades. The circuitry, shown simplified in figure 4.12, is divided into two sections: the automatic gain control section (including the attenuator) and the frequency divider section.

4.39 AUTOMATIC GAIN CONTROL.

4.40 The "C" input signal from the input connector passes through the voltage-controlled attenuator to the RF amplifier. The attenuator consists of two diodes in series with the signal path and three diodes shunting the signal path. With no signal from the AGC amplifier (M1), series diodes CR2 and CR5 are forward-biased providing a low impedance signal path while shunting diodes CR1, CR3, and CR8 are back-biased and provide little attenuation to the signal. As the AGC signal goes negative, series diodes CR2 and CR5 conduct less, increasing their apparent impedance while the diodes in shunt begin conducting and attenuating the signal. The signal from the attenuator passes through the three-stage amplifier (Q3, Q4, and Q5) which increases the signal level to approximately 200 mV rms. The AGC circuit maintains 200 mV rms at the bases of Q11 and Q14.

4.41 The output of the amplifier is applied to the divider section and to a voltage rectifier circuit consisting of diodes CR9 and CR10. The rectifier produces a positive dc voltage level proportional to the RF level of the amplifier output which, after amplification and inversion by differential amplifier M1, controls the attenuator. The gain control circuit holds the signal level of the amplifier input to approximately 50 mV (1 mV with option 030). With option 030, operation is the same as described for the standard Prescaler, but an additional stage of amplification is included (see schematic, figure 6.15).

4.42 FREQUENCY DIVIDER.

4.43 This portion of the Prescaler consists of a discrete transistor flip-flop, a driver circuit (Q18, Q19, and Q20), and a ECL* type D flip-flop, M2. The discrete transistor flip-flop consists of transistors Q6 through Q17. The function of this circuit is to divide the frequency of the signal by two. At low frequency operation, the information is transferred so fast (on the positive edge of the pulse) that it is possible for the flip-flop to go into oscillation at a natural resonate frequency of 300 MHz. A Skew circuit is employed to guard against self oscillation.

4.44 The driver stage for the discrete flip-flop consists of Q8, Q11, Q14, and Q17. The level at which transistors Q8 and Q11 switch is the same at all frequencies. The level at which transistors Q14 and Q17 switch is controlled by the skew circuit consisting of C35, CR16, R55, R59, and C38. The output of the skew circuit is frequency dependent. At frequencies below 300 MHz, the current path is from −18V through resistors R59, R55, and diode CR16 to ground. This biases Q17 at −.2V. Below 300 MHz, the input signal has to overcome the −.2V bias on Q17 base before the flip-flop toggles. As the frequency goes above 300 MHz, the impedance of capacitor C35 decreases and the signal coupled by C35 increases in amplitude. The signal is rectified by CR16. As the frequency continues to increase, capacitor C38 charges to a higher DC level (approaching zero) removing the −.2 volts bias.

4.45 Diodes CR11 through CR14 are level shifters which increase the rise and fall time of the discrete flip-flop. The output of the discrete flip-flop is amplified by Q18, Q19,

*emitter-coupled logic

and Q20. The signal is applied to ECL flip-flop M2. The reset line of M2 is controlled by $\overline{Fc}$. When Frequency C is selected $\overline{Fc}$ is false, M2 is released from the reset state and divides the frequency of the signal by two. The signal (now divided by four) is fed to the input gate of the steering logic. When $\overline{Fc}$ is true, Frequency C is not selected and the flip-flop M2 output is held in the reset state.

4.46 Signal Conditioning Module (Schematic: figure 6.2).

4.47 The Signal Conditioning Module conditions the signal to be compatible with ECL logic and establishes the trigger level of the channel A input. An additional (and basically identical) module is used for conditioning the channel B input.

4.48 In dual-channel models, the input to the channel B Signal Conditioning Module comes from either of two sources depending on the position of the SEP/COM switch. In the COM (common) position, the B input signal is from the channel A input connector (and common with A). In SEP (separate), the signal is from the B input connector (figure 4.13).

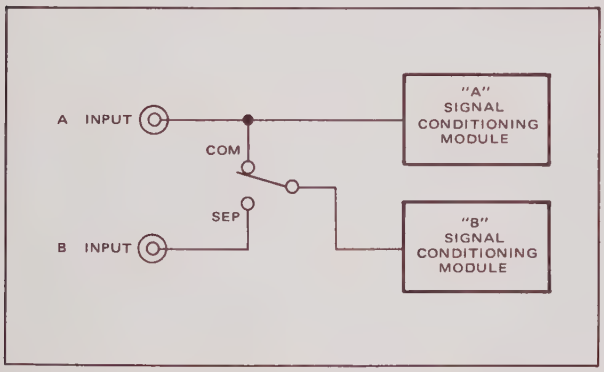


Figure 4.13 - SEP/COM Switch

4.49 Since the modules are identical for channels A and B, only channel A Signal Conditioning is described.

4.50 CHANNEL A ATTENUATOR (figure 4.14).

4.51 With the AC/DC coupling switch set to AC, the signal applied to input A flows through capacitor C1; with DC selected, the capacitor is bypassed through the coupling switch, S207. The signal flows through the attenuator according to the range selected. In the 1-volt range, the signal passes directly through the INPUT VOLTAGE range switch; in the 10-volt range, the signal is attenuated by a factor of 10 (20 dB); and in the 100 volt range, the signal is attenuated by a factor of 100 (40 dB). From the range switch, the signal passes through 100-kilohm resistor R4 in parallel with 47 pfd capacitor C2 to the signal conditioning network.

4.52 SCHMITT TRIGGER.

4.53 As shown in figure 4.14, the signal from the channel A attenuator (f_a in) flows through emitter follower circuits Q1 and Q2. Transistors Q4 and Q8 form a gain stage to drive the input side of a Schmitt trigger consisting of transistors Q3, Q5, Q6, and Q7. The signal from the attenuator is prevented from exceeding ±4 volts by clamp zener diodes CR1, CR2 and diodes CR3 and CR4. The trigger level of the trigger circuit is determined by the potential applied to the input of the follower circuits consisting of Q9 and Q10. With PRESET selected (the extreme counter-clockwise position of the front panel trigger level

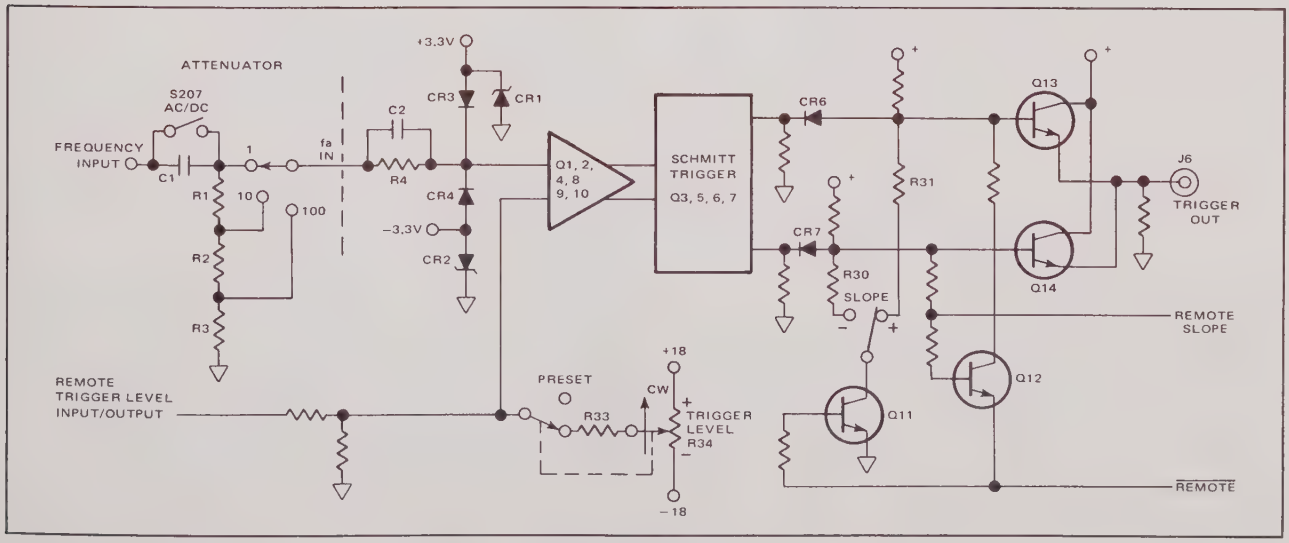


Figure 4.14 - Signal Conditioning Block Diagram

control) and assuming no remote level input, the trigger level is approximately zero volts (0 VDC ± 5% of the input voltage range selected). With PRESET out, the trigger level is adjustable by the trigger level control across ±300% of the range selected. The trigger level may be monitored by connecting a voltmeter across the analog output on the rear panel.

4.54 SLOPE.

4.55 The trigger circuit generates two outputs (180° out of phase) which are gated through diode CR6 or diode CR7, depending on the position of the +/– slope switch. With + slope selected, the anode of diode CR6 is held low through R31 and Q11. A positive pulse is generated during the positive-going edge of the input signal and passes through CR7, through Q14 to connector J6. With – slope selected, the anode of diode CR7 is held low through R30 and Q11. A positive pulse, generated during the negative-going edge of the input signal, passes through CR6 through Q13 to connector J6. When Remote is not selected, transistor Q11 is conducting and the signal that appears at J6 is determined by the position of the +/– (slope) switch on the front panel. In Remote, Q11 is off and Q12 determines the signal at J6.

4.56 Switch Board Assembly (Schematic: figure 6.4).

4.57 The Switch board assembly is one of two large printed circuit boards mounted to the base plate. The Switch board is accessible from the bottom of the counter. The switch board contains the following circuits: reference conditioning and 100 MHz harmonic generator, fast counting decade, counter steering logic, multiplier time base decades and switches, time base steering logic, control logic, and start/stop logic. Each circuit is described in the following paragraphs.

4.58 REFERENCE CONDITIONING CIRCUIT.

4.59 The Reference Conditioning circuitry converts the reference signal to a 10 MHz square wave and routes it to the steering circuits. This circuit processes a reference signal supplied either from the internal frequency source or from an external frequency standard through rear panel connector J106. The source is selected by the rear panel REF switch S102. The internal frequency source is a self-contained, temperature-compensated oscillator located on the Readout board. The external reference (5 or 10 MHz) must be capable of delivering 1 volt RMS at connector J106 (input impedance is 1K ohm). With the REF switch set to the EXT position, an external signal is fed to the input of the conditioning circuitry and the signal path from the internal frequency source is open; with the INT position selected, the internal frequency source is supplied to the input of the conditioning circuitry and the output of the conditioning circuitry is routed to connector J106 for use as a secondary standard source.

4.60 This circuit is shown in simplified form in figure 4.15. The signal from the reference switch is routed to the amplifier consisting of Q12 and Q13. This circuit passes 10 MHz signals or doubles inputs of 5 MHz to 10 MHz. The output of this circuit drives the active 10 MHz crystal filter Y1 which passes only 10 MHz. The active filter output is amplified by Q15 and routed through three NAND (MA1-3, MA1-6, and MB6-11) gates used as in-

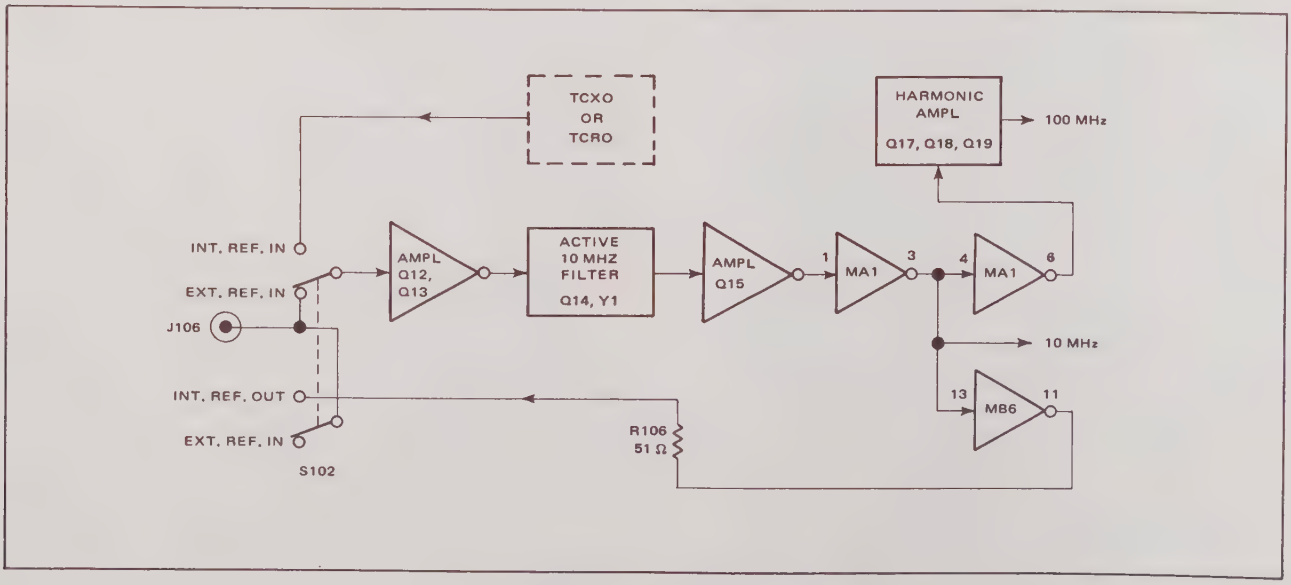


Figure 4.15 - Reference Conditioning Circuit

verters. The output of gate MA1-3 is routed to the Steering circuits of the instrument (10 MHz) and to the input of the other two inverters MA1-4 and MB6-13. The output of gate MB6-11 is fed through 51 ohm impedance matching resistor (R106) to the REF switch S102. When the reference switch is in the EXT position, the 10 MHz is connected to connector J106. The output at MA1-6 is fed to the Harmonic amplifier circuitry consisting of transistors Q17, Q18, and Q19. Transistor Q17 is a frequency multiplier, producing an output of 50 MHz from the harmonics of the 10 MHz input. Transistor Q18 functions as a doubler producing an output of 100 MHz. Transistor Q19 is a 100 MHz amplifier, the output of which is fed to the Timebase Steering circuitry.

4.61 FAST COUNTING DECADE (Figure 6.4).

4.62 The Fast Counting Decade consists of four high-speed counters (MD2, MD3, and MD4) interconnected to form a divide-by-ten circuit. The BCD outputs of the counter are buffered and inverted through transistors Q3, Q4, Q5, and Q6 and routed to the quad latch ME9, driver MF9, and the least-significant digit readout on the Readout board. The buffered 4 and 8 bits from the decade are combined in NAND gate MC5-8 to form a quasi-square output (fa/10) with a frequency equal to 1/10 of the decade input signal. The counter is controlled by a gate signal applied to clock input C1 in the first flip-flop MD2. When C1 is false, the pulses at the clock input C2 are counted; when C1 is true, the flip-flop is inhibited. The gate control line connected to C1 is designated $\overline{\Delta t}$.

4.63 COUNTER STEERING LOGIC.

4.64 This circuitry routes signals to the input of the fast-counting decade according to the measurement mode selected. Signal flow through the circuit is shown in figure 4.16a through c.

4.65 Ratio, Totalize and Frequency A Modes (figure 4.16a).

4.66 Lines from the Ratio, Totalize and Frequency A positions of the FUNCTION switch are applied to a three-input NAND gate, MF5. The line for the selected mode is pulled low by the FUNCTION switch selection. The output of MF5 is high biasing CR1 and CR2 such that the f_a signal flows through CR1 and CR2 to MD1-3. MD1 is a ECL* four-input OR gate. The signal on pin 3 of MD1 causes the output of MD1 to change state (all other inputs to MD1 are low). The signal is routed to the clock input of MD2, a type D ECL flip-flop. Flip-flops MD2, MD3A, MD3B, and MD4 form a divide-by-ten fast-counting decade divider. The output of the fast counting decade drives the display counter on the Readout board and updates the least-significant digit of the readout.

*emitter-coupled logic

4.67 Time Interval Modes (Figures 4.16b and c).

4.68 The signal flow for Time Interval in all multipliers except the one multiplier, is as follows. The Time Interval mode is selected by the FUNCTION switch and $\overline{Ti}$ is pulled to ground. The output of a two input Nand gate MF6-11 goes high. This causes Nand gate ME6-11 output to go low and the three input gate MF5-6 output to go high. This enables a Nand gate ME5-3 to invert the f/n signal and pass $\overline{f/n}$ to ME5-8. Signal $\overline{f/n}$ is connected to R17 and R18 which translates the signal to a ECL Level. The signal is routed to a four input ECL Nor gate MD1-4. The other three inputs to MD1 are low. The output of MD1 is routed to a clock input C2 of the fast counting decade (MD2-8). The time that the counts are allowed to accumulate in the fast counting decade is controlled by $\overline{\Delta t}$ (main gate) applied to clock input C1 of MD2-6.

4.69 The signal flow for Time Interval mode with the "1" multiplier depressed is as follows, figure 4.16c. The Time Interval mode is selected by the FUNCTION switch and $\overline{Ti}$ is pulled to low. The output of a two input Nand gate MF6-11 goes high. The $\overline{1'}$ line is low. This causes Nand gate MF6-3 output to go high. Outputs of gates MF6-11 and MF6-3 are connected to Nand gate MF6-6 inputs. The output of Nand gate MF6-6 is connected to Nand gate MF6-9 and is low. Both inputs to Nand gate MF6-9 are low. The output of Nand gate MF6-8 which is high goes through a RC filter to a 1 Kohm, R15. With the output of Nand gate MF6-8 high, the 100 MHz reference is routed to pin 5 of MD1, an ECL four-input Nor gate.

4.70 Period Mode (Figure 4.16d).

4.71 The signal flow for the Period mode is as follows. Period is selected by the FUNCTION switch and $\overline{Pi}$ is pulled to low. The $\overline{Pi}$ line is connected to a three input Nand gate MF5-4. The output of MF5-6 is high. This enables Nand gate ME5-3. The Scaled output (f/n) is connected to one input of ME5-2. With the other input to ME5-1 high, the f/n is passed through, inverted and connected to Nand gate ME5-9. The other input to ME5-10 is high. The $\overline{f/n}$ signal is inverted and is connected to resistors R17 and R18. These two resistors change the voltage level from a TTL to a ECL level. The output from R17 and R18 is connected to a four input ECL Nor gate MD1. The other three inputs are low on MD1 and the output is connected to the clock input of the fast counting decades (MD2-8).

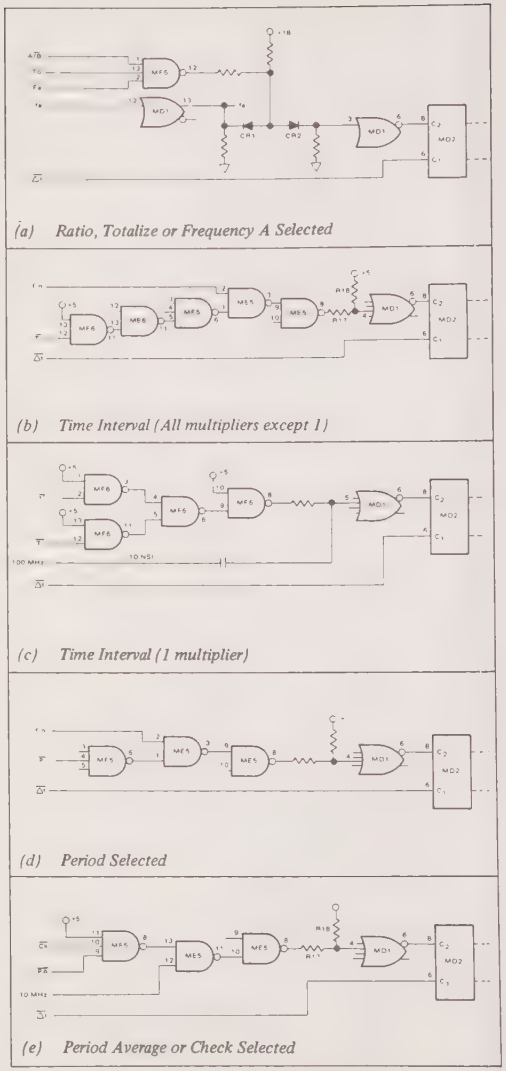

(a) Ratio, Totalize or Frequency A Selected
(b) Time Interval (All multipliers except 1)
(c) Time Interval (1 multiplier)
(d) Period Selected
(e) Period Average or Check Selected

Figure 4.16 - Counter Steering Logic

4.72 Period Average and Check Modes (figure 4.16e).

4.73 Signal flow in Period Average and Check modes are as follows. Period Average or Check is selected by the FUNCTION switch, and one of the two lines, $\overline{PA}$ or $\overline{Ck}$, is pulled to low. $\overline{PA}$ and $\overline{Ck}$ are connected to the inputs of a three-input Nand gate, MF5. The output of MF5-8 is high. The signal from MF5-8 is connected to two-input Nand gate, ME5-13. The other input ME5-12 is connected to the 10 MHz Reference. The output of ME5-11 ($\overline{10\ MHz}$) is connected to the input of a two-input Nand gate, ME5-10. The other input to ME5-9 is high. The output of ME5-8 (10 MHz) is connected to the input of a four input ECL Nor gate, MD1, via a TTL to ECL level translator consisting of R17 and R18. The other three inputs are low. The output of MD1 is routed to the clock input of the fast-counting decades (MD2-8).

4.74 MULTIPLIER TIME BASE SWITCH LOGIC.

4.75 The interlocking pushbutton switches select one of ten decade divider outputs. The time base decades divide the signal applied to the input by 1, 10, 10^2, 10^3, 10^4, 10^5, 10^6, 10^7, 10^8, or 10^9. The outputs are selectable by the MULTIPLIER/TIME BASE switches. The MULTIPLIER/TIME BASE switch selected pulls the line low. The low level is routed to an inverter through a decoupling diode. The high output is connected to a two-input NAND gate. The other input of the NAND gate is connected to one of the ten outputs of the time base decades. If a multiplier of 10^2 through 10^9 is selected, the output signal of the nand gate is routed through a reclocking circuit. The reclocking circuit is necessary to remove the propogation delays developed in the time base decades. The 1 and 10 multipliers are routed around the reclocking circuit via two nand gates. The output of the gate is the frequency applied to the time base decades divided by the multiplier or f/n.

4.76 Signal f/n is used as a start/stop pulse within the counter and delivered to the rear panel as Scaled Out. Signal f/n is always produced with the first pulse applied to the time base decades and the first pulse is not dependent on the multiplier selected. The time base decades are reset to the nine state at the end of display time when $\overline{T^2\ CLEAR}$ goes low. When the first pulse is applied to the time base

decades, the output of the decades changes from all nines to all zeros. Thus, a change of state of output f/n is produced from any one of the ten multiplier switch positions.

4.77 The signal f/n is derived from various input signals to the time base decades. The reference oscillator (10 MHz) is applied to the input of the time base decades in the Check, Frequency A, Period and Time Interval modes. Selection of the MULTIPLIER/TIME BASE switches determines the repetition rate of f/n. Frequency A is applied to the input in Period Average mode. Selection of the switches determines the number of periods of f_a to be measured before f/n is generated. Frequency B is applied to the input in Ratio and Time Interval Average modes. Selection of the switches selects the number of periods of f_b input to be counted before f/n is generated. Frequency A divided by

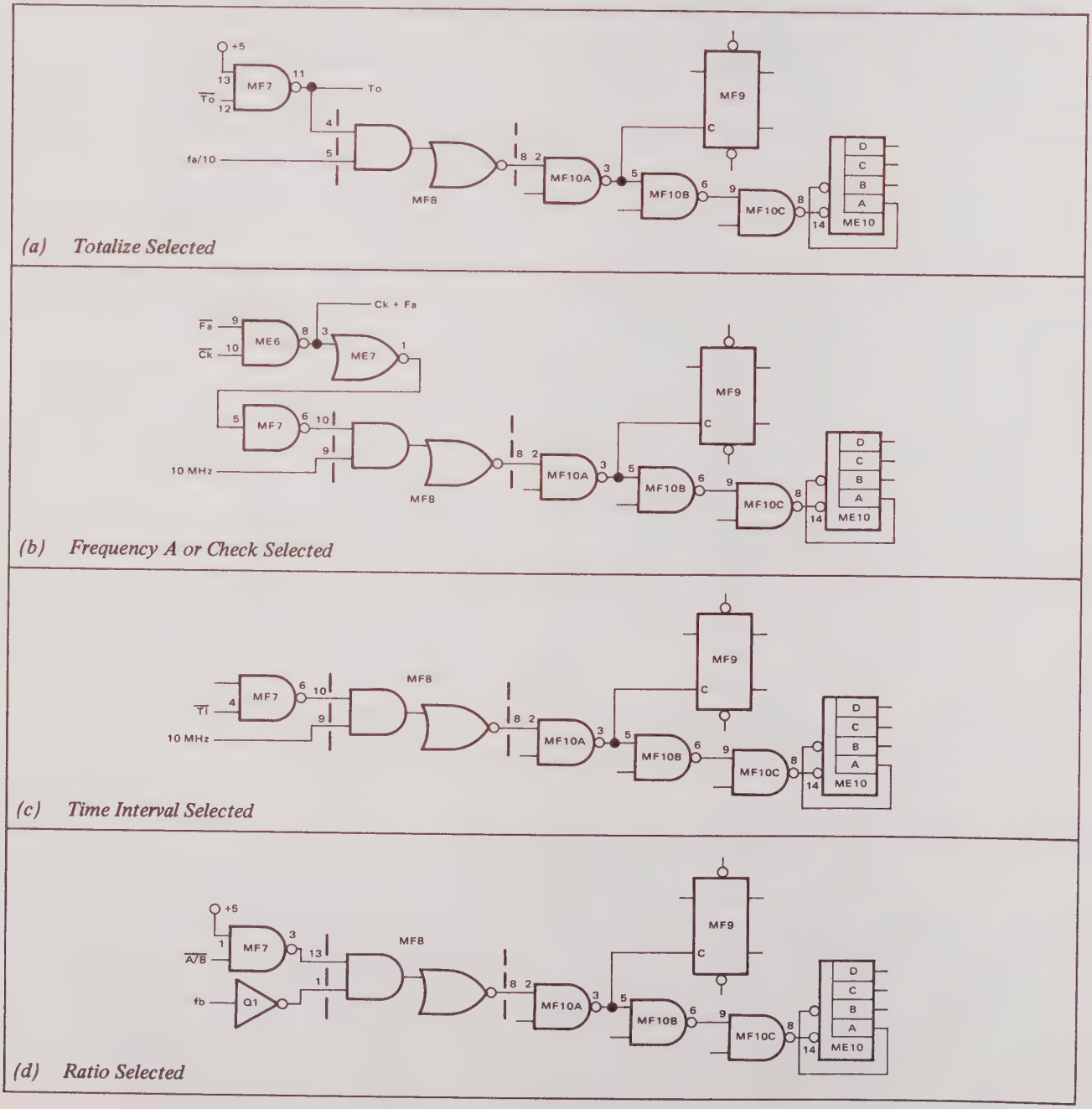


Figure 4.17 - Time Base Steering Logic

continued on page 4-11

ten (f_a/10) is applied to the input in the Totalize mode. Selection of the switches determines the scaling factor of f/n. The reference oscillator divided by four is applied to the time base decades in the Frequency C mode. Selection of the switches determines the repetition rate of f/n. Signal f/n is used for the start/stop pulses which establish the gate time. The reference oscillator is applied to the input of the multiplier/timebase decades in the time interval mode. Signal f/n is ten times faster than what is indicated by the multiplier timebase switch. The decimal point is shifted to the left one place to indicate the correct count. This increases the resolution on this mode to 10 ns.

4.78 TIME BASE STEERING LOGIC (Figure 4.17a - g).

4.79 This circuitry routes signals to the time base divider circuit according to the measurement mode selected. Signal flow through the circuit is shown in figures 4.17a through g.

4.80 Totalize Mode (Figure 4.17a).

4.81 Signal flow through the Time Base Steering logic in the Totalize Mode is as follows. The Totalize mode is selected by the FUNCTION switch and $\overline{To}$ is pulled to ground. $\overline{To}$ is connected through Nand gate MF7 to an expandable 4-wide 2-input Nor gate, MF8. The output of MF8 is routed through Nand gates MF10A, MF10B, and MF10C. The output of MF10C is applied to the clock input to the time base decades (ME10-14).

4.82 Frequency A and Check Modes (Figure 4.17b).

4.83 Signal flow through the Time Base Steering logic in the Frequency A or Check mode is as follows. Frequency A or Check mode is selected by the FUNCTION switch which pulls one of the two lines $\overline{FA}$ or $\overline{Ck}$ low. These two lines are connected to Nand gate ME6. The output of ME6 (Ck + Fa) is connected to Nor gate ME7. The signal (Ck + Fa) is inverted through ME7-1. The output of ME7-1 is applied to Nand gate MF7-5. The output of MF7-6 is tied to pin 10 of a expandable 4-wide 2-input Nor gate MF8. The input of MF8 is high, thus enabling gate MF8. The 10 MHz reference, connected to pin 9 of MF8, passes on through MF10A, MF10B, MF10C to the time base decade clock input ME10-14.

4.84 Time Interval Mode (Figure 4.17c).

4.85 Signal flow through the Time Base Steering logic in the Time Interval mode is as follows. Time Interval is selected by the FUNCTION switch which pulls the TI line low. The $\overline{TI}$ line is connected to the input to Nand gate MF7-4. The other input, being high, causes the output of MF7-6 to be high. The output of MF7-6 is connected to one of two inputs to Nand gate MF8. The other input to MF8-9 is the 10 MHz reference. Since this gate is enabled, the 10 MHz reference passes through to MF10A, MF10B, MF10C, and to the time base decade clock input ME10-14.

4.86 Ratio Mode (Figure 4.17d).

4.87 The signal flow through the Time Base Steering logic in Ratio mode is as follows. Ratio (A/B) is selected by the FUNCTION switch. The switch pulls the A/B line low. The $\overline{A/B}$ line is routed to Nand gate MF7. The output of MF7-3 is high and is applied to pin 13 of MF8. The other input (pin 1) is tied to transistor Q1. When Q1 is turned on, pin 1 of MF8 becomes high and gate MF8 is enabled. The signal, f_b, passes through MF8 to MF10A, MF10B, and MF10C to be counted by the time base decades.

4.88 Period Average Mode (Figure 4.17e).

4.89 The signal flow for the Time Base Steering in Period Average mode is as follows. The Period Average mode is selected by the FUNCTION switch, which pulls the $\overline{FA}$ line low at the input of inverter MD8-13. The output of MD8-12 is connected to one input of Nand gate ME5-4. The other input of ME5 is connected to $\overline{fa'}$. Signal fa' passes through ME5 to MF10A. Nand gate MF10A is enabled and fa' is applied through MF10B and MF10C to the time base decades.

4.90 Frequency C Mode (Figure 4.17f).

4.91 The signal flow for the Time Base Steering in Frequency C mode is as follows. Frequency C is selected by the FUNCTION switch. The FUNCTION switch pulls the control line, $\overline{Fc}$, low. Fc is connected to Nand gates ME6-1, MF7 and MF10B. The output of ME6-3 is high and is connected to Nor gate ME7-2. The output of ME7-1 is connected to Nand gate MF7-5 and is low. The output of MF7-6 is connected to pin 10 of MF8 and is high. The signal flow in Frequency C mode is from MF10A-3 to a type D flip-flop, MF9-11, connected as a divide-by-four counter. The output of MF9-6 is applied through Nand gate MF10D-12 to MF10C-10 and to the time base decades.

4.92 Period Mode (Figure 4.17g).

4.93 The signal flow for the Time Base Steering in the Period mode is as follows. Period is selected by the FUNCTION switch. The FUNCTION switch pulls the control line $\overline{Fi}$ low. $\overline{Fi}$ is connected to Nand gate ME6-2. The output of ME6-3 is high and is connected to Nor gate ME7-2. The output of ME7-1 is connected to Nand gate MF7-5 and is low. The output of MF7-6 is connected to pin 10 of MF8 and is high. This enables the 10 MHz reference on pin 9 of MF8 to pass through MF8 to Nand gates MF10A, MF10B, and MF10C to the time base decades input ME10-14.

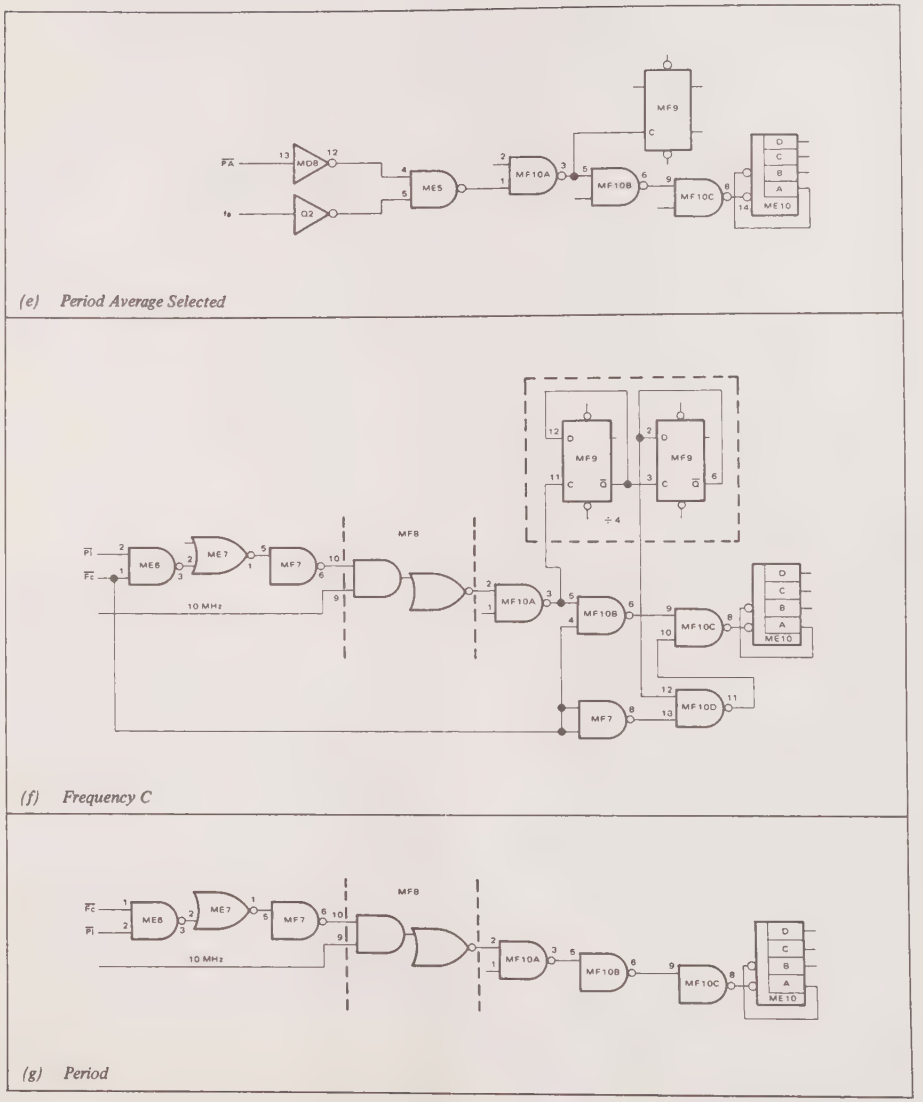


Figure 4.17 - Time Base Steering Logic

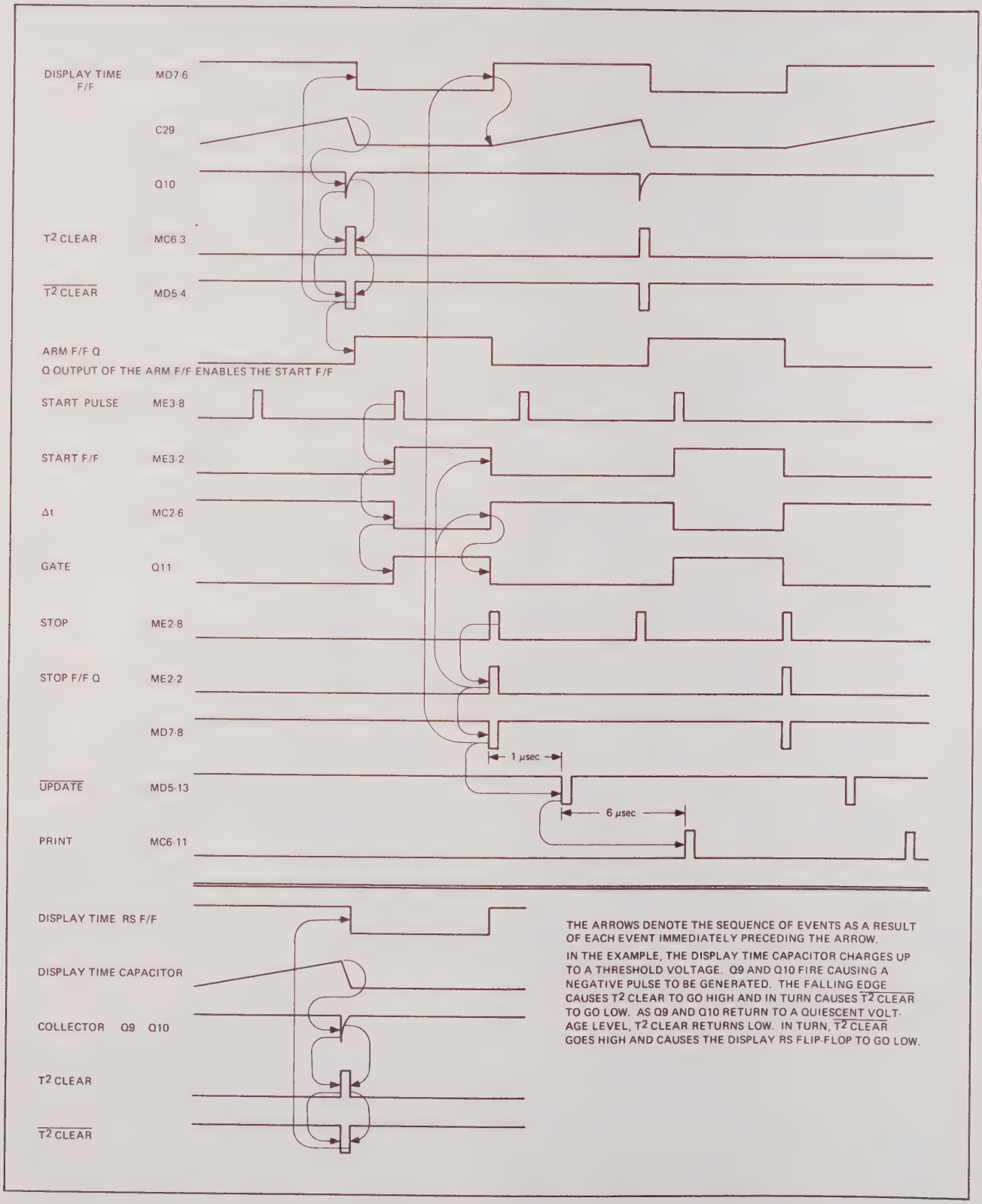

DISPLAY TIME F/F
MD7·6
C29
Q10
T2 CLEAR
MC6·3
T2 CLEAR
MD5·4
ARM F/F Q
Q OUTPUT OF THE ARM F/F ENABLES THE START F/F
START PULSE
ME3·8
START F/F
ME3·2
Δt
MC2·6
GATE
Q11
STOP
ME2·8
STOP F/F Q
ME2·2
MD7·8
1 μsec
UPDATE
MD5·13
6 μsec
PRINT
MC6·11
DISPLAY TIME RS F/F
DISPLAY TIME CAPACITOR
COLLECTOR Q9 Q10
T2 CLEAR
T2 CLEAR
THE ARROWS DENOTE THE SEQUENCE OF EVENTS AS A RESULT OF EACH EVENT IMMEDIATELY PRECEDING THE ARROW.
IN THE EXAMPLE, THE DISPLAY TIME CAPACITOR CHARGES UP TO A THRESHOLD VOLTAGE. Q9 AND Q10 FIRE CAUSING A NEGATIVE PULSE TO BE GENERATED. THE FALLING EDGE CAUSES T2 CLEAR TO GO HIGH AND IN TURN CAUSES T2 CLEAR TO GO LOW. AS Q9 AND Q10 RETURN TO A QUIESCENT VOLTAGE LEVEL, T2 CLEAR RETURNS LOW. IN TURN, T2 CLEAR GOES HIGH AND CAUSES THE DISPLAY RS FLIP-FLOP TO GO LOW.

Figure 4.18 - Control Logic Timing

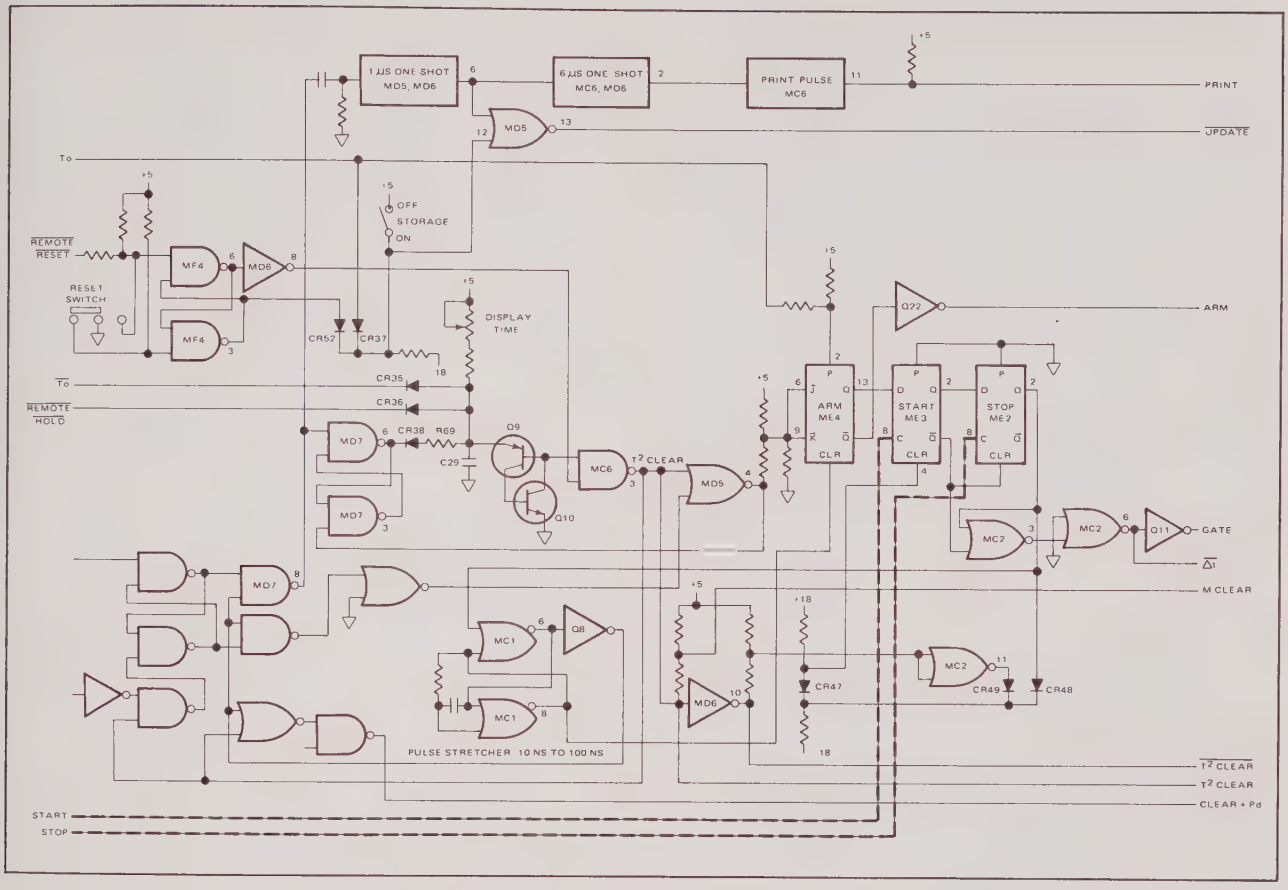


Figure 4.19 - Block Diagram Control Logic

4.94 CONTROL LOGIC.

4.95 This circuitry controls the timing sequence for the balance of the instrument; it generates the main gate control signal ($\overline{\Delta t}$). The timing sequence is illustrated in the timing diagram of figure 4.18, the circuitry is shown simplified in figure 4.19. With the DISPLAY TIME control set to produce periodic readings (not in the HOLD position), the operating sequence for all modes, except Totalize, begins when MD7-6 goes high. The display time integrating capacitor C29 charges at a rate dependent on the setting of the DISPLAY TIME control. When the voltage across C29 reaches approximately +3.7 volts, a latching circuit (Q9 and Q10) fires. The output of gate MC6-3 goes high (T^2 CLEAR) and Nand gate output MD5-4 goes low resetting the display time RS flip-flop (MD7). The voltage across C29 is discharged through R60 and CR38. The display time circuit is reset, and MC6-3 goes low. From the previous measurement, ME4-13 Q is low, ME3-2 Q is low, and ME2-2 Q is low. An inverted T^2 Clear pulse from MC6-3 is fed to the input of ME4-6, 9 setting ME4-13 high on the trailing edge of the pulse from MC6-3. The instrument is now "armed" and prepared to take the next measurement.

4.96 A START pulse to ME3-8 (clock) sets ME3-2(Q) high which enables ME2 so it will respond to the next STOP pulse. The START pulse also causes $\overline{\Delta t}$ to go low (MC2-6) and MAIN GATE to go high (Q11). When a STOP signal is received at ME2-8 (clock) ME2-2 goes high resetting ME3-2 low via the clear input on ME3-4 through diodes CR48 and CR47, and causing $\overline{\Delta t}$ to go high and MAIN GATE to go low terminating the count. The STOP flip-flop output ME2-2 also generates a pulse through a one-shot pulse stretcher (10 ns to 100 ns) MC1-8 resetting ME4-13 low via the clear input ME4-12. A pulse from the one-shot through Q8 and MD7-8 resets the Display time RS flip-flop low (MD7-6) and fires the 1 microsecond one-shot MD5 and MD6. The one-shot output (MD6-6) passes through MD5-13 to produce the $\overline{\text{UPDATE}}$ and the pulse is applied to the input of a 6 microsecond one-shot. The 6 microsecond one-shot output (MD6-2) is inverted to form the PRINT pulse used with Systems Interface, Option 008.

4.97 In the Totalize mode, the operation of the circuitry is the same with the following exceptions: the selection of Totalize sets MD5-12 high through CR37, causing gate MD5-13 output to go low which is $\overline{\text{UPDATE}}$. This allows

the accumulation of pulses in the counter to be continuously monitored by the operator. Also, the Preset input pin 2 of ME4 is held high presetting the Q output ME4-13 high, and the display time circuit is held low through diode CR35 and is disabled. The Start and Stop pulses are generated manually by the START/STOP switch on the front panel or electrically through the external gate line EXT. GATE and performs the same functions as the internally generated pulses in the other measurement modes. However, since ME4-13 is held high as long as the instrument is in the Totalize mode, the totalize measurement may be started and stopped as many times as desired.

4.98 The reset circuit (MF4) is used to reset the Counting Decades to zero. In REMOTE HOLD or HOLD, for modes other than Totalize, the reset commands one new reading and holds the reading. In Totalize, the reset circuit resets the counting decades to zero and stops the count. The START/STOP switch must be pressed to start the count again.

4.99 START/STOP LOGIC (Figures 4.20a – e).

4.100 The Start/Stop logic gates the proper pulses to the START and STOP flip-flops in the control logic to control the duration of the main gate. The control logic must "arm" before a START or STOP pulse will be accepted by the Start and Stop flip-flops. The control logic sets the Arm flip-flop which enables the Start flip-flop. The control logic is now ready to accept the START pulse. In all modes except Time Interval and Ratio both a Start and a Stop pulse are gated to the control logic simultaneously. The control logic disregards the stop pulse until the Start flip-flop has been set. When the Start flip-flop is set the Stop flip-flop is enabled and the Start flip-flop is disabled. When the Stop pulse arrives, the Stop flip-flop sets. Again, both the Start and Stop pulses are gated to the control logic simultaneously. The control logic now disregards the Start pulse. In Time Interval and Ratio modes, the Start and Stop pulses are not both gated to the control logic at the same time. The start pulse originates from the signal f_a and usually occurs first. The Stop pulse originates from the signal f_b and occurs after signal f_a. The START initiates the main gate and the STOP terminates the main gate. The routing of the signals is shown in figures 4.20a through e.

4.101 Totalize Mode (Figure 4.20a).

4.102 In the Totalize mode the start pulse is initiated by the START/STOP switch or by the external gate input connected to REMOTE. The START/STOP switch and the EXT. GATE line are tied to the input of an RS flip-flop (MF4) made from two cross-coupled nand gates. The output of the flip-flop is low when the START/STOP switch is in its normal position. When the switch is depressed, the

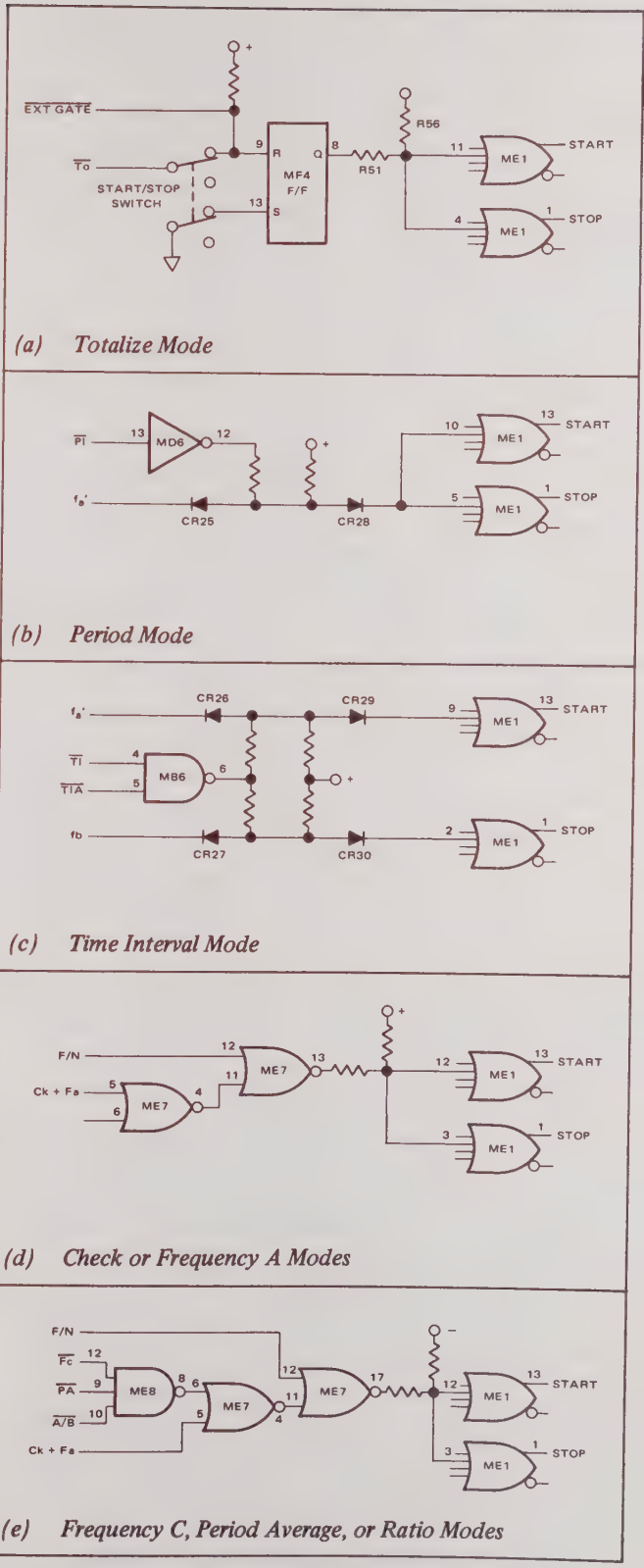


Figure 4.20 - START/STOP Signal Flow

inhibit is removed and the flip-flop output goes high. The output stays high as long as the switch is depressed and returns low when the switch is released. The start pulse is initiated when the Start/Stop switch is pressed or the external gate line is connected to REMOTE. The output of the RS flip-flop goes high. The signal goes through a TTL to ECL level translator consisting of R51 and R56. The ECL signal is routed to ECL Nor/Or gates ME1-11 and ME1-4. The output of the Nor/Or gate ME1-13 goes to produce a start pulse for the control logic. The next time that the Start/Stop switch is pressed or EXT. GATE is pulled to REMOTE, another pulse will be produced and detected in the control logic as a stop pulse.

4.103 Period Mode (Figure 4.20b).

4.104 In the Period mode, the $\overline{Pi}$ line is low causing inverter MD6-12 output to be high. This enables the diode gate CR25 and CR28. The diode gate is tied to ECL NOR/OR gates ME1-10 and ME1-5. Note: see Section 5 for Diode Gate Theory. On the rising edge of Frequency A trigger (fa') the output of Nor/Or gate ME1-13 rises to produce a START pulse for the control logic. On the next rising edge of Frequency A trigger, the output of Nor/Or gate ME1-1 goes high and produces a STOP pulse for the control logic.

4.105 Time Interval Mode (Figure 4.20c).

4.106 In the Time Interval mode, the $\overline{TI}$ line is low. $\overline{TI}$ is inverted through ME6-6. The output of ME6-6 enables two diode gates made up of CR26, CR29, and CR27, CR30. When Frequency A triggers, a positive pulse is produced (fa'). Signal fa' is connected via diode gate CR26 and CR29 to ECL Nor/Or gate ME1-9. The output of ME1-13 goes high producing a start pulse and is routed to the control logic. When Frequency B triggers, a positive pulse is produced (f_b). Signal f_b is connected via diode gate CR27 and CR30 to a ECL Nor/Or gate ME1-1. The output of ME1-1 goes high producing a STOP pulse which is routed to the control logic.

4.107 Check or Frequency A (Figure 4.20d).

4.108 In Check or Frequency A mode, Ck + Fa is high and is connected to Nor gate ME7-5. The output of ME7-4 is low and enables Nor gate ME7-13. The scaled output or f/n is connected to ME7-12. At the start of the gate the signal f/n goes low and causes the output of Nor gate ME7-13 to go high. The output of ME7-13 causes the outputs of two four input ECL Nor/Or gates to go high. Or gate ME1-13 output causes the start flip-flop in the control logic to set. The next time that f/n goes low a positive pulse is produced (STOP) at ME1-1. The stop pulse is routed to the control logic and sets the stop flip-flop.

4.109 Frequency C, Period Average, and Ratio Modes (Figure 4.20c).

4.110 In the Frequency C, Period Average, and Ratio modes, one of the input lines (Fc, PA, A/B) to Nand gate ME8-8 is selected and pulled low. The output of ME8-8 is high disabling Nor gate ME7-4. The output of ME7-4 is low enabling Nor gate ME7-13. Scaled Out f/n is gated through to a TTL to ECL level change and to ECL Nor/Or gates ME1-13 and ME1-1. The gate is initiated when f/n goes low. The output of ME7-13 goes high and is routed through the TTL to ECL level translator to the Or gate ME1-13 and on to the control logic as a START pulse. The next time f/n goes low, the output of ME7-13 goes high and is routed through the TTL to ECL level translator and to ECL Or gate ME1-1 and on to the control logic as a STOP pulse. The output of ME1-13 is the start pulse and the output to ME1-1 is the stop pulse.

4.111 MARKER LOGIC (Figure 4.21).

4.112 The MARKER output provides a negative 18-volt pulse starting when channel A triggers and stopping when B triggers. It is used for increasing the intensity of an oscilloscope trace.

4.113 This circuit consists of an emitter coupled JK flip-flop (MF3) driving inverter Q20. A trigger pulse from channel A (f_a') sets the Q output of the flip-flop MF3 high resulting in an output of approximately minus 18 volts. A trigger pulse from the channel B input (f_b) sets Q of the flip-flop to low causing the transistor to saturate and producing a marker output of about zero volts.

4.114 Readout Board (Figure 6.5).

4.115 The readout board assembly is one of two large printed circuit boards mounted to the base plate. The readout board is accessible from the top of the counter. The readout board contains the following circuits; the reference

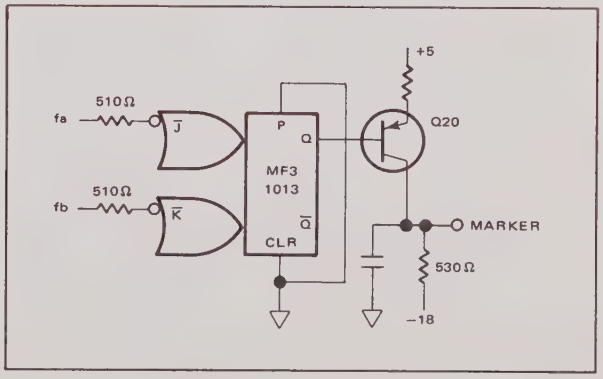


Figure 4.21 - Marker Logic

oscillator, the power supply, the function switch, the display tubes, the TTL counting decades, and the storage.

4.116 COUNTER/DISPLAY (Figure 6.6).

4.117 The counter and display circuit counts, stores and displays the number of pulses received from the high-speed decade on the switch board. The counter consists of seven decade counters (type 7490), eight quadruple bistable latches (type 7475), eight numeric display tube drivers (type 7441), and eight numeric display tubes. An additional tube, driver, latch, and decade are included in instruments having the 9th digit, Option 004. Transistor Q1 controls the update inputs of all the quad latches. A low update signal from the control logic allows each latch to assume the same level as the decade counter to which it is connected. A high update signal allows the latches to store the information. The $\overline{T2}$ CLEAR line (when low) resets the decade counters to zero.

4.118 POWER SUPPLY.

4.119 The power supply (figure 4.22) provides all voltage levels for the operation of the instruments and standby power (with power OFF selected) for the continuous operation of the optional frequency source (with instruments equipped with Option 200). All supplies except the +150 volt supply are regulated.

4.120 The +150V supply is used by the gas tube display and derived from a +250 volt full wave bridge circuit. Current limiting resistor R60 drops the voltage to the tubes to approximately +150 volts when the tubes are conducting. With power OFF, the +150 line is opened.

4.121 The +28 volt supply is used only for the optional frequency reference (Option 200) and is derived from a tapped secondary full wave rectified circuit and discrete 28-volt regulator.

4.122 The −18-volt supply is used throughout the instrument and is derived from a −28 volt full wave rectified supply and a regulator consisting of zener CR20 and transistors Q26 and Q101. Referring to the schematic, Q26 and CR20 (18 volt zener) form a 12 milliamp current generator with resistors R66 and R67 supplying current to the zener. The base of Q101 is driven by the current generator causing Q101 to conduct heavily pulling the output towards −28 volts through diode CR22. At −18 volts, diode CR21 starts conducting causing the current generator to lessen the output and at this point stability is reached. When the power switch is set to OFF the −18 volt supply is shorted to ground. The voltage at the cathode of CR22 turns off

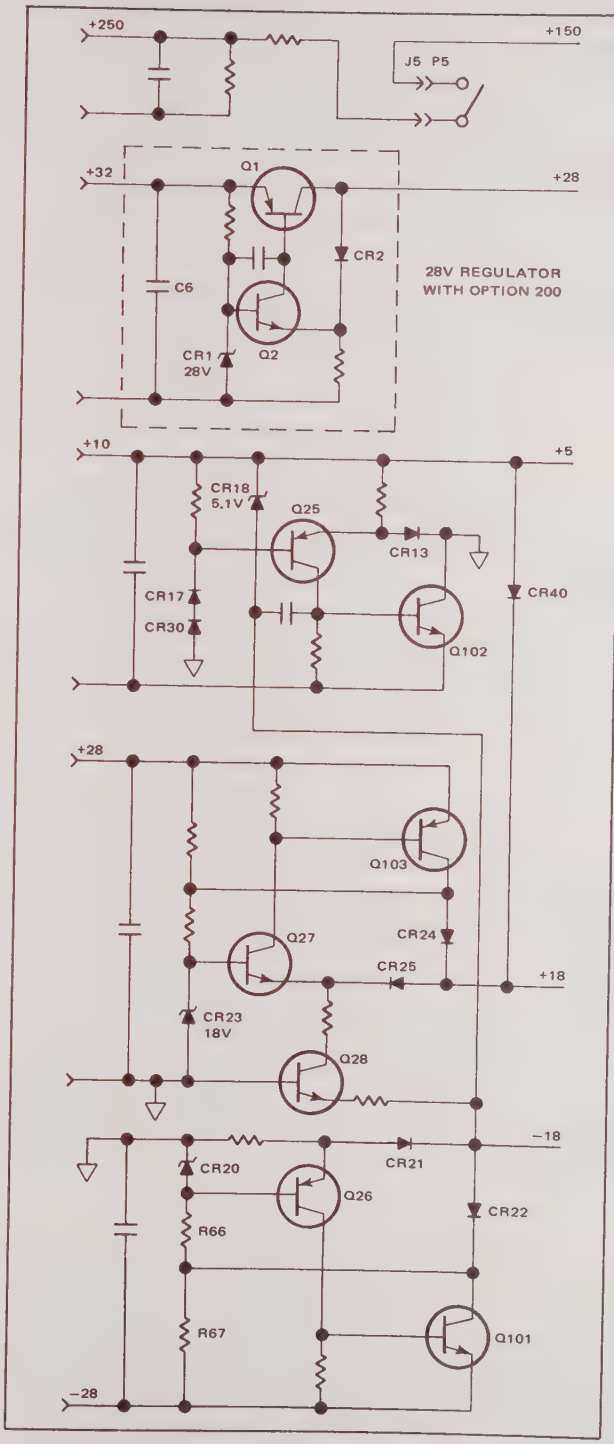


Figure 4.22 - Power Supply

Q26 by depriving CR20 of idling current and the short circuit current folds back to approximately 8 ma as shown in figure 4.23.

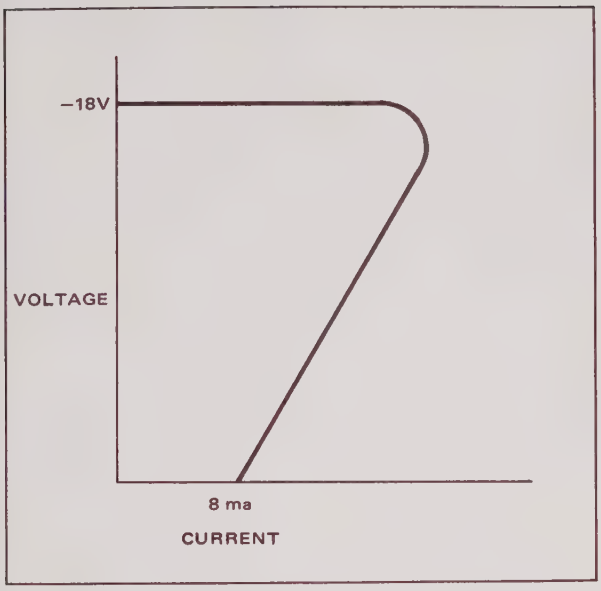


Figure 4.23 - Characteristic of −18V Regulator

4.123 The +18 volt supply is also used throughout the instrument and is derived from a +28 full wave rectified circuit. The regulator circuit, consisting of transistors Q27, Q28, Q103, and 18 volt zener CR23, operates in the same manner as the −18 volt supply. Transistor Q28 functions as a switch and turns off the +18 supply when the −18 volt supply goes to ground (instrument is shut off).

4.124 The +5 volt supply is used by all of the digital circuitry. The regulator operates in the same manner as the ±18 volt supplies but uses a 5-volt zener. The current for the zener is supplied through resistor R63 from the −18 volt supply.

SECTION 5 MAINTENANCE

5.1 INTRODUCTION.

5.2 This section contains maintenance information for the counter. Included are TTL theory, ECL theory, diode gate theory, signal flow in all modes of operation, troubleshooting, and diagrams to localize, isolate and locate defective components. Performance check procedures are not included in this section, but can be found in Section 3.

5.3 RECOMMENDED TEST EQUIPMENT.

5.4 Test equipment recommended for maintaining, troubleshooting, and servicing the counter is listed in table 5.1. Test equipment with equivalent characteristics may be substituted for equipment listed.

5.5 CALIBRATION.

5.6 Internal Reference Oscillator Adjustment.

5.7 The following procedures are given for adjustment of the counter's internal reference oscillator. One of three different reference oscillators may be used in the counter. The reference oscillators are as follows:

a. Standard Temperature-Compensated Crystal Oscillator (TCXO); Dana part number 730551

b. Option 050 Temperature-Compensated Crystal Oscillator (TCXO); Dana part number 730578

c. Option 200 Temperature-Compensated Reference Oscillator (TCRO); Dana part number 730228

5.8 For standard and option 050 reference oscillators, perform the following set-up procedures.

a. Set the counter controls as follows:

Control	Setting
DISPLAY TIME	about 9 o'clock
FUNCTION	FREQ A
TIMEBASE	10 second
A Slope	Plus (+)
A Coupling	DC
A Trigger Level	PRESET
SEP/COM	SEP
STORAGE	ON
REF	INT OUT
A Input Voltage Range	10

Table 5.1 - Required Equipment

Instrument Type	Required Specification	Recommended Instruments
Frequency Standard	1 MHz, 5 MHz, or 10 MHz	
Oscilloscope	150 MHz Bandwidth 500 MHz Bandwidth	TEK 454 TEK 7900
Voltmeter	10 mVDC to 200 VDC	Dana 4300
Sine Wave Generator	2 Hz – 10 MHz	Dana 7010
VHF Signal Generator	10 – 150 MHz	HP8654A
VHF Signal Generator	1 – 550 MHz (Not required for 8015B)	HP8654A
Alignment Tool	.075" Hex (nonmetallic)	General Cement 9300
Alignment Tool	Blade (nonmetallic)	
Sampling Voltmeter	0 – 600 MHz	HP3406
BNC "T" connector		
50Ω Tee connector		HP 10221A
2 – BNC to GR Adaptors		

b. Connect a 1 MHz frequency standard to A input.

c. Allow 1 hour time for the counter temperature to stabilize.

d. The difference between the internal reference oscillator and the 1 MHz frequency standard can be determined by the following formula:

Internal Oscillator Frequency = (20,000,000 – Counter Reading). See table 5.2.

Table 5.2 - Reference Oscillator Error

Counter Display	Internal Reference Osc.
999.9950 kHz	10000.050 kHz
999.9975 kHz	10000.025 kHz
1000.0000 kHz	10000.000 kHz
1000.0025 kHz	9999.975 kHz
1000.0050 kHz	9999.950 kHz

5.9 ADJUSTMENT PROCEDURE – STANDARD TCXO.

a. Apply power to the counter for one hour before attempting TCXO adjustment (see paragraph 5.8). Remove the top cover (see paragraph 5.19, "Access to P.C. Boards"). Locate the TCXO located on the Readout assembly near the rear of the counter (see figure 6.5, Readout Layout). Remove the #6 metal or nylon cap screw on the top of the reference oscillator. Use a nonmetallic alignment tool for adjustment. Some oscillators require a hexagon .075 dia. alignment tool, and others require a blade type.

b. Insert the proper adjustment tool into the #6 screw hole on the top of the reference oscillator. Adjust the TCXO until the display reads 1000.0000 kHz. Wait ten seconds and readjust the TCXO if the first adjustment was not correct. Remove the adjustment tool.

c. After the initial adjustment, replace the cap screw and the top cover. Allow 30 minutes for temperature stabilization and recheck the reading.

5.10 ADJUSTMENT PROCEDURE – OPTION 050 TCXO.

5.11 Allow the counter to temperature stabilize for one hour before adjustment and verify one hour after adjustment. Follow the procedures outlined in paragraph 5.9.

5.12 ADJUSTMENT PROCEDURE – OPTION 200 TCRO.

5.13 The object of the following procedures is to determine short term drift of the TCRO as well as to adjust the frequency. The adjustments are the COARSE and FINE controls on the rear panel. *Use only a non-metallic blade type adjustment tool for these adjustments.*

a. Set the counter controls as described in paragraph 5.8a.

b. Allow the counter to temperature stabilize for 72 hours before calibration. (It is not necessary to turn the power on during the warmup and stabilization period. The TCRO is an oven oscillator which operates from a separate +28 volt supply.) Set DISPLAY TIME to about 9 o'clock one hour before adjustment.

c. Connect a 1 or 5 MHz Frequency Standard to channel 1 of a dual channel oscilloscope. Trigger the oscilloscope on channel 1 only. Set the oscilloscope sweep rate to .02 μs per cm.

d. Connect a BNC cable to the counter INT OUT connector J106 on the rear panel. Set the REF switch S102 to the INT OUT position. Connect the other end of the BNC cable to the second channel of the oscilloscope. The oscilloscope display should indicate a stationary and a moving waveform. The moving waveform is the counter reference oscillator.

e. Remove the nylon cap screws. Adjust the COARSE adjustment (rear panel, see figure 6.8) and then the FINE adjustment until as near a completely stable waveform as possible is obtained. The channel 2 waveform will be drifting to the left or right. If the channel 2 waveform is moving to the left, the internal reference oscillator is higher in frequency than the frequency standard. If the channel 2 waveform moves to the right, the internal reference oscillator is lower in frequency than the frequency standard.

f. To determine the drift rate, measure the time it takes the oscilloscope pattern to drift the width of one cycle on channel 2. Note: 1 cycle equals 5 divisions on the oscilloscope. The oscillator drift can be determined from figure 5.1.

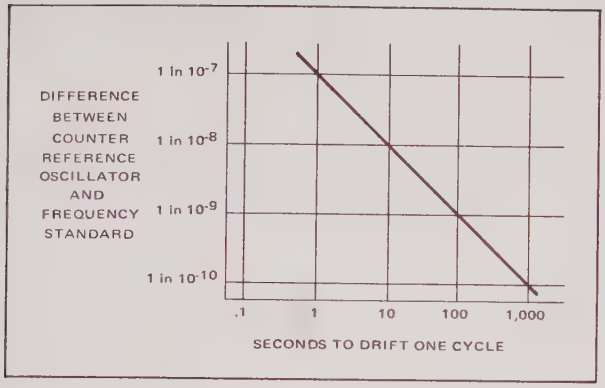


Figure 5.1 - Oscillator Drift

5.14 REFERENCE ADJUSTMENT (10 Nanoseconds)

a. Connect scope between the emitter of Q18 and ground at TP8, see Switch Board Layout, figure 6.3. Adjust C54 for the waveform in figure 5.2.

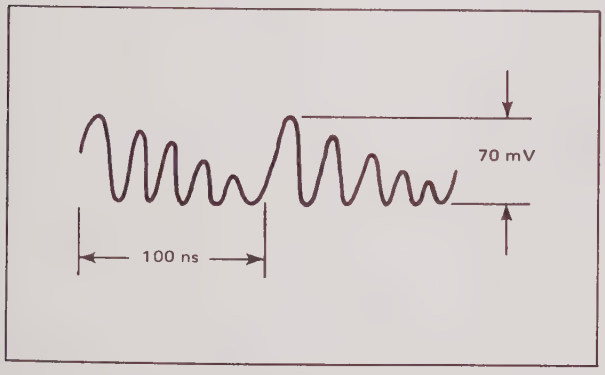


Figure 5.2 - 5th Harmonic Output

b. Connect scope between reference output at E7 and ground (E8). Adjust C56 located near MC1 for a 100 MHz signal of an amplitude greater than 600 mV peak-to-peak. See waveform in figure 5.3.

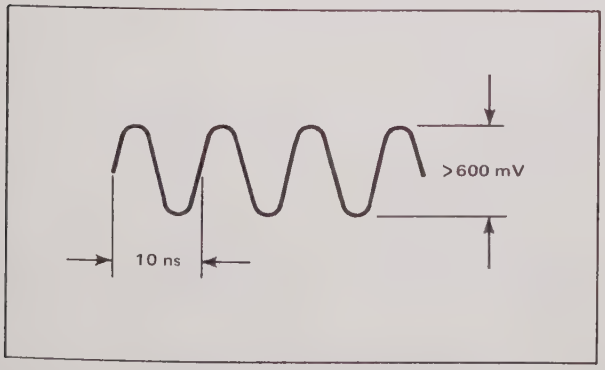


Figure 5.3 - 100 MHz Signal

5.15 SIGNAL CONDITIONING CALIBRATION – CHANNEL A.

a. Set the controls as follows:

Control	Setting
A Slope	(+) Plus
A Coupling	AC
MULTIPLIER/TIMEBASE	1 second
A Trigger Level	PRESET
A Voltage Input Range	1
SEP/COM	SEP
FUNCTION	FREQ A
DISPLAY TIME	about 9 o'clock

b. Apply power to the counter 1 hour before adjustment. Do not remove the top or bottom covers during warmup.

c. Apply a 10 MHz 100 mV rms signal to channel A input. Use a DC coupled oscilloscope with .5V/cm sensitivity to compare logic levels at MD1-12 and MD2-8 on the switch board assembly. Refer to figure 6.3, Switch Board Layout, for locations.

d. Adjust the ECL level pot R17A (figures 5.5 and 6.1) so the logic levels at MD1-12 are the same as the logic levels at MD2-8.

e. Connect a 150 MHz, 40 mV RMS signal to channel A input.

f. While observing the signal at MD1-12, switch the channel A slope between (+) plus and minus (–). Note the DC voltage shift between + and – slopes. Adjust the offset pot R20A for a minimum DC shift. Notice that with no DC shift, a permissible change in peak-to-peak amplitude may occur. The signal at MD1-12 is shown in figure 5.4. The signal output in either slope must be a minimum of .4 volts peak-to-peak.

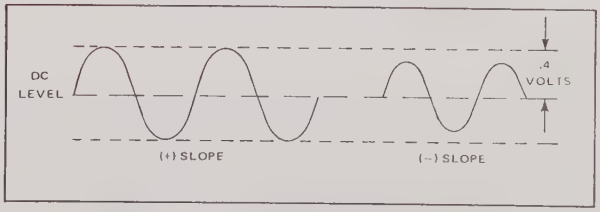


Figure 5.4 - Signal Conditioner Output

h. Check the sensitivity over the band in both + and – slopes. Nominal sensitivities are as follows:

50 mV RMS to 100 MHz, 100 mV RMS to 150 MHz.

g. Place channel A in – slope. Increase signal level to insure that the proper reading is displayed by counter. Incrementally decrease input signal level until an improper reading is observed. Then adjust R17A for the correct reading. Continue this process until maximum sensitivity is obtained.

i. Final check and adjustment should be completed after the unit is at ambient temperature with the top and bottom covers on.

5.16 SIGNAL CONDITIONING CALIBRATION – CHANNEL B.

a. Set the Controls as follows:

Control	Setting
Slope A	+
Slope B	–
Coupling A	AC
Coupling B	AC
Trigger Level A	PRESET
Trigger Level B	PRESET
Input Range A	1
Input Range B	1
SEP/COM	SEP
FUNCTION	TI
DISPLAY TIME	about 9 o'clock
MULTIPLIER/TIMEBASE	1 second

b. Apply power to the counter 1 hour before adjustment. Do not remove top and bottom covers during warmup period.

c. Apply a 10 MHz 100 mV rms signal to channel A input. Apply the same signal to a 10 dB Attenuator. Connect the output of the attenuator to channel B input.

d. Monitor the signal output of signal conditioner at ME1-2 on the Switch Board assembly. (figure 6.3)

e. Use a DC coupled oscilloscope with .5V/cm sensitivity and compare logic levels at ME1-1 and ME1-2 on the Switch board.

f. Adjust the ECL level control R17 (figures 5.5 and 6.1) such that the logic levels at ME1-1 are the same as the logic levels at ME1-2.

g. Incrementally decrease input signal level until an improper reading is observed. Then adjust R20 for the correct reading. Continue this process until maximum sensitivity is obtained.

h. Check the sensitivity over the band in both + and – slopes. Nominal sensitivities are: 0 – 10 MHz, 50 mV rms.

i. Final check and adjustments should be completed after the counter is at ambient temperature with both top and bottom covers on.

5.17 PERIODIC MAINTENANCE.

5.18 To determine if the counter is operating properly within specifications, perform the performance check (Section 3).

5.19 ACCESS TO PC BOARDS.

5.20 To remove top and bottom covers, proceed as follows:

a. Remove power cord.

CAUTION

The power supplies are still active as long as the power cord is plugged into the power AC source.

b. Loosen the four captive screws, one at each corner of the top cover and remove the top cover.

c. Turn the counter upside down. Loosen the four captive screws on the bottom cover and remove the bottom cover.

5.21 PCB REMOVAL.

5.22 When removing the printed circuit board for replacement, repair, and servicing, always remove the AC power cord before disassembly. Refer to figure 5.25, page 5-15 for assembly location.

5.23 RF Assembly (Not in 8015B) (figure 6.12 or 6.14).

a. Remove the six #4 phillips-head screws around the outer edge of the assembly.

b. Disconnect the two subminiature RF connectors.

c. Disconnect P10 at the rear of the counter.

d. On instruments having option 030, remove the five #4 screws holding the RF shield on the component side. Remove shield.

> NOTE
> The R.F. assembly is very sensitive to component movement. Do not move any components or recalibration will be necessary.

5.24 Signal Conditioning Assembly (figure 6.1).

a. Remove the trigger level knobs and the input range knobs.

b. Remove the two #6 phillips-head screws on the top of the signal conditioner and one #6 phillips-head screw on the bottom.

c. Remove the subminiature R.F. connectors.

d. Remove the two #6 phillips-head screws holding cable clamps on the cable between the signal conditioner and P9. Remove P9 and remove the assembly.

e. To service the attenuator switch, remove the four #4 phillips-head screws located at each corner of the printed circuit board. The printed circuit board can be moved away from the switch assembly for servicing.

5.25 Readout Assembly (figure 6.5).

a. Remove the interconnection printed circuit assembly from J4.

b. Remove P1 at the left rear of the assembly.

c. Remove P5 and the FUNCTION knob at the right front side.

d. Remove the seven #6 phillips-head screws (one in the center and six around the perimeter of the board). The Readout assembly can now be removed.

5.26 Switch Board Assembly (figure 6.3).

a. Remove the interconnection printed circuit assembly from J2.

b. Unscrew the subminiature RF connectors from the Signal Conditioning assembly and the RF assembly.

c. Remove P3 from J3.

d. Remove the six #6 phillips-head screws, two in the center and four around the perimeter of the printed circuit board. Remove the switch board assembly.

5.27 COMPONENT REPLACEMENT.

5.28 When replacing a circuit board component, use a low heat soldering iron (25 watt). Heat must be used sparingly as damage to the circuit foil may result. Plated-thru holes may be cleaned with a solder remover while heat is applied. The connection should be cleaned with a cleaning solution after the component removal and replacement.

5.29 Integrated Circuit Replacement.

5.30 Integrated circuits can be unplugged and substituted without soldering or assembly removal. The use of special tools to remove IC is not recommended. To remove an IC, place both thumbs on top of the IC and both index fingers at the ends of the IC. Gently rock the IC upward in small steps. Do not "pop" it out in one motion. To replace an IC, be sure the notched end points the same direction as the other ICs on the board. Straighten any bent pins. Align the pins on the IC with the holes in the socket and press the IC in firmly using one or two fingers.

5.31 Identification of Parts.

5.32 All parts are listed in the parts list, Section 7, by assembly. Reference designators are called out on the schematic and can be found on the layout drawings. The Dana part number and description are given in the parts list. All integrated circuits used in the counters are standard 7400 series TTL and ECL that can be purchased from your local supplier. Special parts may be obtained from Dana by writing or calling Product Service at our toll free number 800-854-3288 or 714-833-1234 collect in California.

5.33 Parts Location.

5.34 The integrated circuits on the Readout and Switch board assemblies are layed out on a grid pattern. Looking at the readout or switch board from the front, the ICs are numbered across the board from left to right, 1 through 12; top to bottom, A through F. Other components are designated by circuit and can be located by the schematic and layout drawing.

5.35 TROUBLESHOOTING.

5.36 This section describes methods for identifying counter troubles and determining the specific corrective action that should be taken. Familiarity with the Operation (Section 3) and Theory of Operation (Section 4) makes troubleshooting easier.

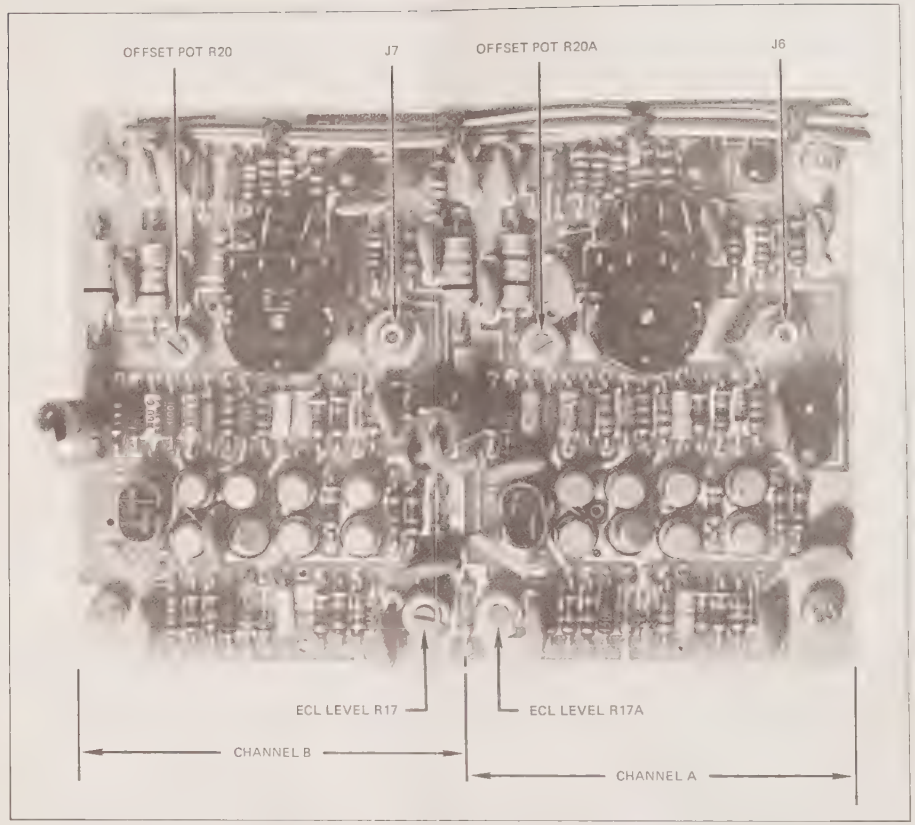


Figure 5.5 - Signal Conditioning Adjustments

5.37 A malfunction can be rapidly defined to one of four categories.

a. Apparent trouble which is really a misplaced control setting or an erratic external signal.

b. Visual damage such as printed circuit board broken, etc.

c. Analog trouble which requires troubleshooting and component replacement.

d. Digital trouble which requires troubleshooting and IC replacement.

5.38 Repairs which require replacement of soldered-in components can be accomplished rapidly, but caution should be taken against soldering with improper procedures. Solder damage to the printed circuit boards is not covered by Dana's warranty.

5.39 Apparent Troubles.

5.40 Apparent troubles are those which appear to be equipment malfunctions, but are really controls which are misadjusted.

5.41 The counter will not operate if a function is incorrectly selected. For instance, if the unknown frequency is connected to input C and FREQ A function is selected, there will be no reading. Be sure the FUNCTION switch is in the proper mode. If the function has been changed, depress RESET to start a new reading in the new function.

5.42 If the input voltage range or trigger level are improperly set, inputs A or B will not operate. Be sure that a measurable signal is present and that controls are set properly for that signal.

5.43 When input C is used (not in 8015B), the automatic gain control will inhibit readings of signals which are less than 50 mV and greater than 1V RMS. Signals will be inhibited if they are outside the measurable band (1.0 MHz to 550 MHz). With Option 030, the automatic gain control will inhibit readings of signals which are less than 1 mV and greater than 1V RMS. Signals will be inhibited if they are outside the measurable band for Option 030 (10 MHz to 500 MHz).

5.44 Due to the sensitivity of input C, open leads which might act as an antenna can cause improper readings. If open leads or probes must be used, it may be necessary to insert a low-pass filter at the counter input to discriminate against unwanted signals received through radiation. Unshielded input signals can cause unwanted signals to override the desired signal. The proper operation of input C can be verified by connecting a signal generator directly to the counter through a shielded 50-ohm terminated cable. Once proper counter operation has been verified, unwanted external signals can be attenuated with a low-phase filter.

5.45 Visual Check.

5.46 A possible source of malfunction could be short or open circuits which disable portions of the counter or load down the power supply, or both. Often these short-circuits can be located by visual inspection. A quick visual check of the counter with the covers removed may reveal foreign metal parts, frayed cable braid, discolored components, etc. which can be easily corrected. Visual checks can be more meaningful after the trouble has been localized.

5.47 Open circuits can also be located visually. Examine connector and wire harnesses for obvious breakage or opens.

Table 5.3 - Front Panel Symptoms

Type of Problem	Refer to Paragraph:
Readout	5.50
Remote Operation	5.65
Self-Check Mode	5.69
Period Mode	5.71
Period Average Mode	5.73
Frequency A Mode	5.75
Frequency C (Not in 8015B)	5.78
Totalize Mode	5.81
Time Interval Mode	5.83
A/B (Ratio) Mode	5.86

5.48 Front Panel Symptoms.

5.49 Localize the trouble to one of the categories listed in table 5.3; then proceed to the appropriate paragraph and follow the suggested procedure.

5.50 READOUT INOPERATIVE.

5.51 If the readout tubes and annunciators do not light, a failure in the 150V supply is indicated. Check the line fuse. It should be .75 amp, 3 AG. If in doubt, measure the AC source at the power transformer T101 to assure that power is getting to the counter. Check the 150-volt supply as follows.

a. Turn power off; remove the power cord at the rear of the counter. The supplies are still active even with the power switch turned off. Remove the top cover and reconnect the power cord.

b. Connect a voltmeter to either side of resistor R60, 3.9K, 3W (figure 6.5). Connect the other lead of the voltmeter to ground (negative side of capacitor C7). The voltage should read about 150 volts DC.

c. Note the action that occurs when the DISPLAY TIME switch is moved clockwise from the PWR OFF position. If the voltage goes very low or to zero, there is a short in the 150V line. If no voltage is present at either side of R60, check the following: R61 (located under C6), C5, CR5 through CR8, and T101.

d. Remove P1 and check for 180 volts rms at points P1-E (blue transformer lead) and P1-D (violet transformer lead).

e. If the high voltage is still not present, check the wire harness for opens or shorts. If no opens or shorts are found, T101 may be defective.

f. If the high voltage is present, reconnect P1 and recheck the 150 volt lines. If the 150 line loads down, locate and eliminate the short on the readout board.

5.52 READOUT TUBE BLURRING.

5.53 If all readout tubes blur, a faulty +5-volt supply voltage is indicated. The 5-volt supply is affected by the other power supplies, so they must all be checked.

5.54 Series regulator transistors for the +5-volt and ±18-volt supplies are mounted on a heatsink on the rear panel. A short to ground in the −18-volt supply turns off the +5-volt and +18-volt supplies. Instruments equipped with Option 200 have a separate +28-volt supply and regulator. A short in this supply also affects the other voltages. It can be measured at J4-X.

5.55 Check the power supply voltages at the points listed below. Refer to figure 6.6 for voltage levels within the power supply.

Power Supply	Measurement Point (figure 6.5)
+5V	J4-20 or CR40 anode
+18V	Cathode of CR40
−18V	Anode of CR22

5.56 If any of the power supply voltages are abnormal, disconnect the load to isolate the trouble to the supply or to the load. If the voltage returns to normal, reconnect the load and selectively unplug the interconnection board, the signal conditioning board, and the prescaler until the source of the overload is located.

5.57 If the trouble appears in only one readout tube, a bad integrated circuit (IC) driver or a bad readout tube is indicated. Driver IC's are 7441's in Row F directly behind the readout tubes. Remove power, and exchange the 7441 behind the bad readout with the neighboring driver. If the trouble moves with the driver (7441), replace the 7441 driver. If the trouble stays when the driver is moved, replace the readout tube. If none of the above solves the problem, inspect the circuit near the tube, driver, or quad latch (7475) for shorts or opens.

5.58 ANNUNCIATORS INOPERATIVE.

5.59 The "gate" and units annunciators are located in front of and below the readout tubes (figure 6.5). They are operated from the +150-volt and +5-volt power supplies. If none of the annunciators light, the power supply is probably faulty. Perform the power supply checkout procedures described in paragraph 5.51.

5.60 If the GATE annunciator does not operate, proceed as follows:

a. Set DISPLAY TIME counterclockwise, just short of the PWR OFF position.

b. Set FUNCTION switch to the CHECK mode.

c. Depress the 100 ms TIMEBASE switch (the GATE light should flash at approximately 130 ms intervals).

d. With an oscilloscope, check at the cathode of CR1 for a pulse going from zero to +4.0 volts. If the pulse is not present, check at J2-4 (see circuit, figure 5.6).

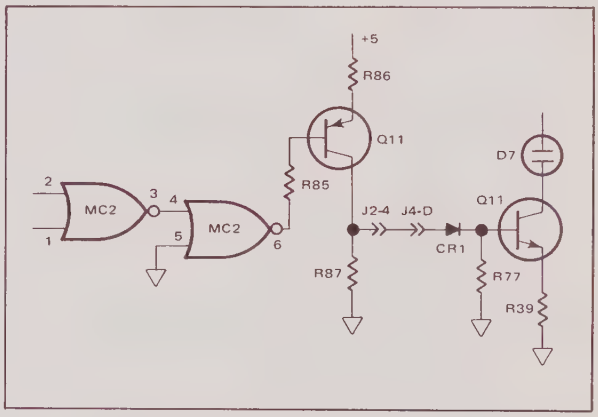


Figure 5.6 - Gate Annunciator

e. If the pulse is not present at J2-4, check the control logic on the Switch board assembly. Verify first that a "start" pulse is being generated.

5.61 If one of the units annunciators does not light, refer to table 5.4. In the table, voltage levels at the inputs and output of gates are listed. If a level differs by ±10% from that listed, the trouble is located between the correct level and the incorrect level. Integrated-circuit drivers in each circuit may be unplugged and exchanged with one of the same type known to be good. If a driver becomes shorted, the corresponding annunciator remains "on". If the driver is open, the annunciator remains "off".

5.62 DECIMAL POINT MALFUNCTION.

5.63 Should any one decimal point not turn on, perform the following decimal point check:

a. Set the FUNCTION switch to FREQ C. Select the 1 μs timebase. No decimal point should be lit. If one is lit, try substituting the readout with the one

Table 5.4 - Units Annunciators Troubleshooting

Annunciator	Function	Select Timebase/Multiplier	Measurement Point	Normal Level	Figure No.
μsec	PERIOD Mode	1 μs	E54 MB11-8	≥2.0 volts	5.7
			MB11-10 MC12-8	≤0.8 volts	
			MB11-11 MB12-3	≥2.0 volts	
			MB12-1	≤0.8 volts	
			MB12-2	≤0.8 volts	
msec	PERIOD Mode	10 μs	E50 MD10-12	≥2.0 volts	5.8
			MD10-13 MD12-8	≤0.8 volts	
			MD12-2	≥2.0 volts	
			MD12-3	≥2.0 volts	
nsec	PER AVG Mode	10^6	E52 MD11-11	≥2.0 volts	5.9
			MD11-13 MC11-8	≤0.8 volts	
			MD11-12	≥2.0 volts	
			MD11-8	≥2.0 volts	
sec	PERIOD Mode	10 ms	E51 MD11-3	≥2.0 volts	5.10
			MD11-1 MC11-6	≤0.8 volts	
			MC11-2	≥2.0 volts	
			MC11-3	≥2.0 volts	
KHz	FREQ A Mode	10s	E53 MB12-8	≥2.0 volts	5.11
			MB12-9 MB12-6	≤0.8 volts	
			MB12-4	≥2.0 volts	
			MB12-5	≥2.0 volts	
MHz	FREQ A Mode	1s	E49 MD10-2	≥2.0 volts	5.12
			MD10-1 MC9-8	≤0.8 volts	
			MC9-1 MA12-6	≥2.0 volts	
			MA12-5 MB8-3	≥2.0 volts	
			MB8-1	≥2.0 volts	
			MB8-2	≥2.0 volts	
			MC9-13	≥2.0 volts	

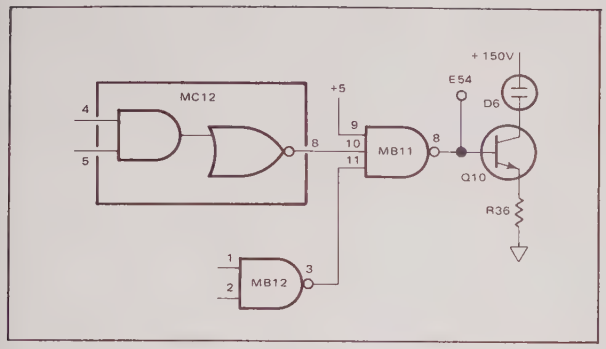


Figure 5.7 - "μsec" Annunciator

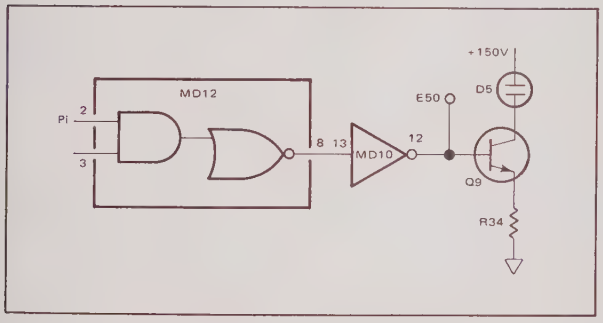


Figure 5.8 - "msec" Annunciator

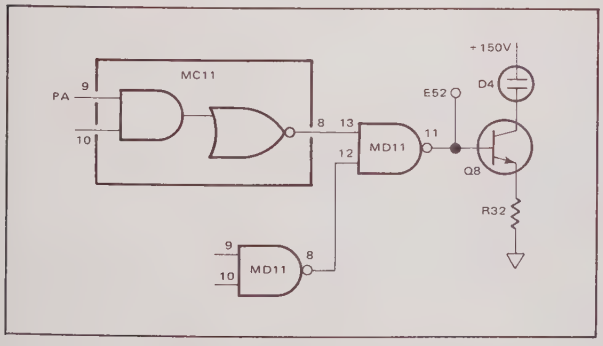


Figure 5.9 - "nsec" Annunciator

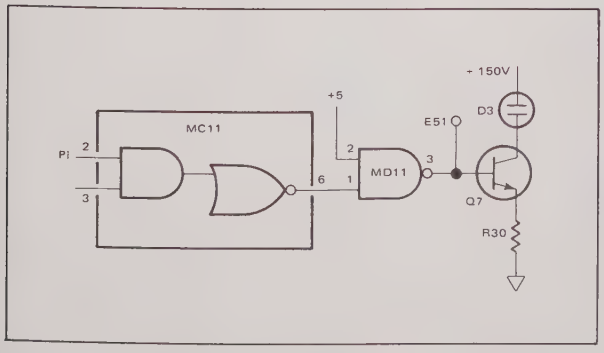


Figure 5.10 - "sec" Annunciator

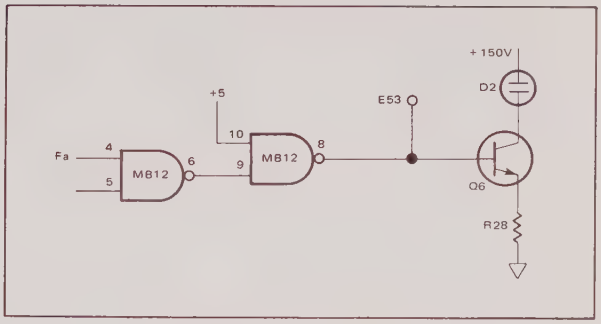


Figure 5.11 - "KHz" Annunciator

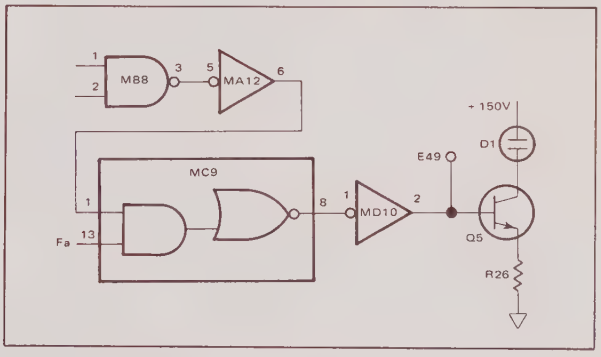


Figure 5.12 - "MHz" Annunciator

next to it. Each decimal point is driven by a transistor which, if open or shorted, causes a decimal point to remain off or on continuously.

b. Depress the 10 μs to 100s TIMEBASE switches; the decimal point should light as shown in table 5.5.

5.64 Procedures for signal tracing through the DP logic are listed in table 5.6.

Table 5.5 - Decimal Point Placement

Timebase	Decimal Point Display								
	V9	V8	V7	V6	V5	V4	V3	V2	V1
10 μs	0	0	0	0	0	0	0	0	.0
100 μs	0	0	0	0	0	0	0	.0	0
1 ms	0	0	0	0	0	0	.0	0	0
10 ms	0	0	0	0	0	.0	0	0	0
100 ms	0	0	0	0	.0	0	0	0	0
1s	0	0	0	.0	0	0	0	0	0
10s	0	0	.0	0	0	0	0	0	0
100s	0	.0	0	0	0	0	0	0	0
Decimal Point	↑	DP8	DP7	DP6	DP5	DP4	DP3	DP2	DP1

Models with Option 004 (9th digit)

Table 5.6 - Troubleshooting Procedure - DP Logic

Decimal Pt.	Select Timebase	Measurement Point(s)	Normal Level	Figure No.
DP1	10 μs	E70 MC7-6	≥2.0 volts	5.13
		MC7-5 MA9-8	≤0.8 volts	
		MA9-4 MA9-5	≥2.0 volts	
DP2	100 μs	E71 CR26 anode CR27 anode	≥2.0 volts	5.14
		MC7-11	≥2.0 volts	
		MC7-12 MC8-6	≥2.0 volts	
		MC7-13 MB9-8	≤0.8 volts	
		MB9-4 MB9-5	≥2.0 volts	
DP3	1 ms	E72 MB7-12	≥2.0 volts	5.15
		MB7-13 MC9-6	≤0.8 volts	
		MC9-4 MC9-5	≥2.0 volts	
DP4	10 ms	E73 MB7-6	≥2.0 volts	5.16
		MB7-5 MA10-8	≤0.8 volts	
		MA10-4 MA10-5	≥2.0 volts	
DP5	100 ms	E74 MB7-4	≥2.0 volts	5.17
		MB7-3 MB10-8	≤0.8 volts	
		MB10-2 MB10-3	≥2.0 volts	
DP6	1s	E75 MC7-8	≥2.0 volts	5.18
		MC7-9 MC10-6	≤0.8 volts	
		MC10-2 MC10-3	≥2.0 volts	
		MC8-8 MC7-10	≥2.0 volts	

Table 5.6 - Troubleshooting Procedure - DP Logic (continued)

Decimal Pt.	Select Timebase	Measurement Point(s)	Normal Level	Figure No.
DP7	10s	E76 MB7-2	≥2.0 volts	5.19
		MB7-1 MC10-8	≤0.8 volts	
		MC10-1 MC10-13	≥2.0 volts	
		MA12-12	≥2.0 volts	
DP8	100s	E77 MB7-10	≥2.0 volts	5.20
		MB7-11 MC8-3	≤0.8 volts	
		MC8-1 MC8-2	≥2.0 volts	
		MA7-10	≥2.0 volts	

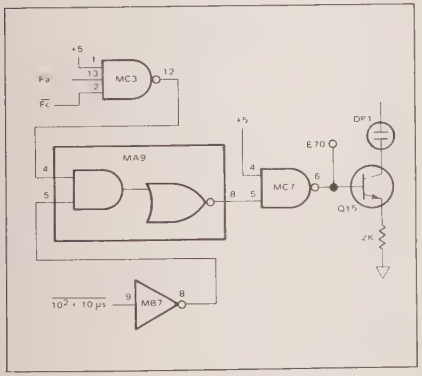


Figure 5.13 - DP1 Decimal Point Logic

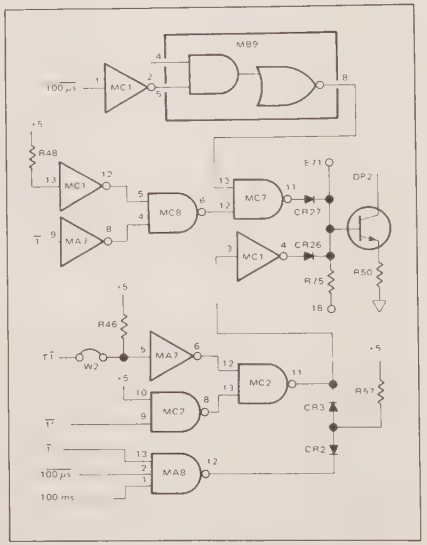


Figure 5.14 - DP2 Decimal Point Logic

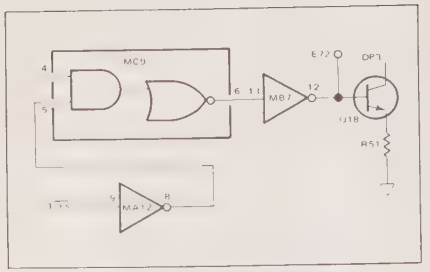


Figure 5.15 - DP3 Decimal Point Logic

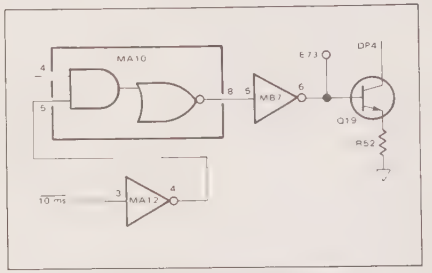


Figure 5.16 - DP4 Decimal Point Logic

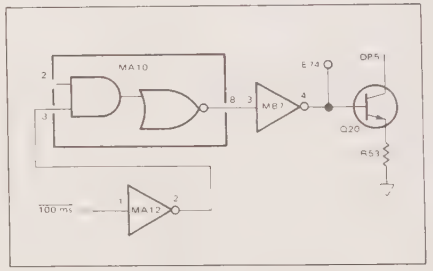


Figure 5.17 - DP5 Decimal Point Logic

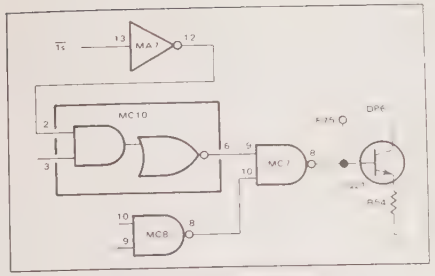


Figure 5.18 - DP6 Decimal Point Logic

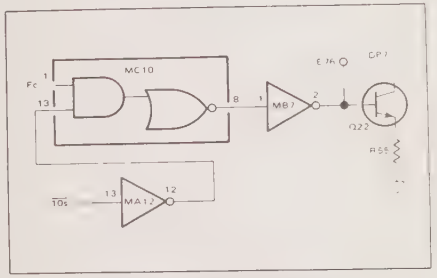


Figure 5.19 - DP7 Decimal Point Logic

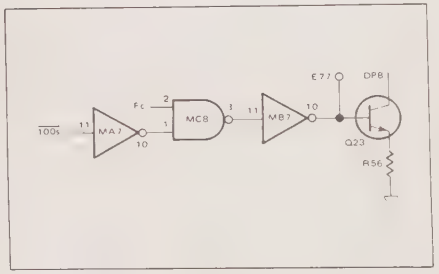


Figure 5.20 - DP8 Decimal Point Logic

5.65 Faulty Remote Operation.

5.66 Normally, problems occurring with the remote programming option occur also in local operation. Verify that transistor Q7 and Q21 on the Switch board turns off with REMOTE selected. If Q7 and Q21 operates properly, a malfunction can be traced by following the procedures for troubleshooting a specific operating mode. Also verify that there are no opens or wiring errors in the external circuits.

5.67 Faulty Operation In One Mode.

5.68 Figures 5.27 through 5.34 show the signal flow through the instrument in each mode of operation. Logic levels are given at significant check points to assist in signal tracing. These figures are at the end of this section.

5.69 CHECK MODE (Figure 5.27).

5.70 In Check mode, the reference oscillator frequency is routed to the counting decades and to the timebase decades.

5.71 PERIOD MODE (Figure 5.28).

5.72 The signal in the Period mode is routed through the Attenuator and the Signal Conditioning assembly where the trigger slope and trigger level are selected. The signal (f_a) is routed to the Control Logic which controls the time that the counting decades are allowed to count the Reference Oscillator or a frequency division of the Reference Oscillator. Follow the procedure in paragraph 5.77. If the signal is present at E2 and E1, refer to the Period Signal Flow schematic for gate levels and signal flow.

5.73 PERIOD AVERAGE MODE (Figure 5.29).

5.74 The signal in Period Average mode is routed through the Attenuator to the Signal Conditioning assembly and to the Multiplier Timebase Decades. The output of the Timebase Decades (f/n) goes to the start/stop logic and on to the Control Logic which controls the counting decades. The Reference Oscillator is routed to the fast counting decades. The counting decades are controlled by $\overline{\Delta t}$. $\overline{\Delta t}$'s time is determined by f_a and the multiplier selected on the front panel. Follow the procedure in paragraph 5.77. If the signal is present at E_1 and E_2, refer to the Period Average Signal Flow schematic for gate levels and signal flow.

5.75 FREQUENCY A MODE (Figure 5.30).

5.76 The signal for Frequency A mode is routed through the Signal Conditioning assembly where the trigger slope and trigger point are selected. Attenuation of the signal also takes place in the attenuator section of the signal conditioning. Frequency A (f_a) is routed to the counting decades. The time that the counting decades are allowed to count is controlled by the Reference Oscillator, Timebase Decades, and the Control Logic. Be sure that the FUNCTION switch is positioned to FREQ A and that the range and trigger level controls are set correctly.

5.77 Connect an oscilloscope to E1* and E2 on the Switch board assembly. Connect a signal to the Frequency A input and adjust the counter accordingly. An ECL square wave should be seen varying between 3.4V and 4.2 volts dc. Try moving the trigger level control over its range. If no signal is found, the trouble is in the Attenuator or Signal Conditioning Module. Refer to the schematic of the Signal Conditioning module for troubleshooting (figure 6.2).

5.78 FREQUENCY C MODE (Figure 5.31, not in 8015B).

5.79 Frequency C is much like Frequency A operation. The signal is connected to the Frequency C input and routed into the Frequency C RF Assembly. The signal is amplified. The amplification is controlled by an automatic gain control circuit (AGC). The signal is divided by two through a discrete flip-flop and divided again by two through a ECL flip-flop. The signal is routed to E3**and E4 on the Switch board assembly. The signal (f_c) goes to a ECL gate and to the counting decades. The Reference Oscillator is gated through to a divide-by-four flip-flop to the Timebase Decades.

5.80 To determine if the Frequency C signal reaches the Switch board, connect an oscilloscope to E4 and E3 on the Switch board. Set the FUNCTION switch to FREQ C. Connect a signal to Input C. A ECL square wave should be seen on the oscilloscope varying between 3.4V and 4.2 volts dc. If no signal is found, the trouble is in the Frequency C RF assembly. Refer to figure 6.12 or 6.13 or figures 6.14 and 6.15 for Option 030 (1 mV, 10 MHz – 500 MHz) for the schematic of the RF assembly.

5.81 TOTALIZE MODE (Figure 5.32).

5.82 The signal in the Totalize mode is routed through the A input to the Attenuator and Signal Conditioning Module where the trigger level and slope are selected. The output of the Signal Conditioner is gated to the counting decades. The counting decades are controlled by the manual start/stop circuit which develops $\overline{\Delta t}$, the gate time for the

*E1 fa signal input
E2 fa signal low

**E3 fc signal input
E4 fc signal low

count. The input signal divided by 10 ($f_a/10$) is routed to the Timebase Decades and to the scaled output connector for external use.

5.83 TIME INTERVAL MODE (Figure 5.33).

5.84 The signals in the Time Interval mode are routed through the A and B inputs to the A and B Signal Conditioning Modules. The Signal Conditioning circuits determine the trigger points and trigger slope. The output of A is at E1 and E2 on the Switch board. The output of B is at E5* and E6 on the Switch board. The Reference Oscillator is gated to the Multiplier Timebase Decades. The Multiplier Timebase Decades are gated to the counting decades. The counting decades are controlled by the Control Logic which is controlled by the stop/start logic. The signal from input A determines the start time and the input B signal determines the stop time. The start and stop circuits define the gate time.

5.85 Verify that the input controls are set correctly. Observe E1 and E2, and E5 and E6 to determine that a square wave pulse is being generated at the correct time. If a signal is not present, refer to the Signal Conditioning schematic, figure 6.2.

5.86 A/B (RATIO) MODE (Figure 5.34).

5.87 The signals in the Ratio mode are routed through the Inputs A and B. The signal from Input A goes to the Attenuator and Signal Conditioning circuits where the trigger level and slope are selected. The output of the A Signal Conditioner (f_a) is routed to the counting decades. The output of B Signal Conditioner (f_b) is routed to the Multiplier Timebase Decades and to the Control Logic. The Control Logic starts and stops the counting decades.

5.88 Verify that there is a signal at the output of the A Signal Conditioner (E1, E2). Verify that there is also a signal at the output of the B Signal Conditioner (E5, E6). If either of these signals are missing, refer to the Signal Conditioner schematic, figure 6.2.

5.89 Troubleshooting The Signal Conditioning Assembly.

5.90 For disassembly refer to paragraph 5.24. Follow the calibration procedures in paragraphs 5.15 and 5.16 (dual channel). If this does not reveal the problem, refer to the schematic, figure 6.2. Voltage levels and signal level are given on the schematic.

5.91 Channel A and channel B are schematically the same. The reference designators are suffixed with an "A" in the channel A circuits. To verify that Q1 and Q10 are matched to each other, proceed as follows:

a. Ground the bases of Q4 and Q8.

b. Measure between the bases of Q2 and Q9. Verify the operation of R20; the voltage should vary from negative, through zero, to positive. If this voltage range cannot be obtained, either Q1 and Q10 are not matched or there is a component failure in the circuit.

5.92 The following pairs of transistors in this circuit are matched as indicated.

Q4 and Q8; V_{be} (base-to-emitter voltage)

Q2 and Q9; V_{be} (base-to-emitter voltage)

Q1 and Q10; R_{ds} (resistance, drain-to-source)

5.93 Troubleshooting The RF Assembly.

5.94 For disassembly, refer to paragraph 5.23. Note: *Do not move any components unless that component is known to be defective.* The RF Assembly is very sensitive to component location. Recalibration will be required if a component is replaced in a critical area. Voltage levels are given on the schematic figures 6.13 or 6.15. However, it is recommended that the RF assembly be returned to Dana's Product Service for repair and calibration.

5.95 BASIC LOGIC DEFINITION.

5.96 TTL Logic.

5.97 A majority of the integrated circuits used in the 8000B counters are TTL type integrated circuits. TTL circuits operate up to ≅15 MHz. The basic Nor function is shown in figure 5.21. Logic levels are:

Logical 0: ≤.8V Logical 1: ≥2.0V

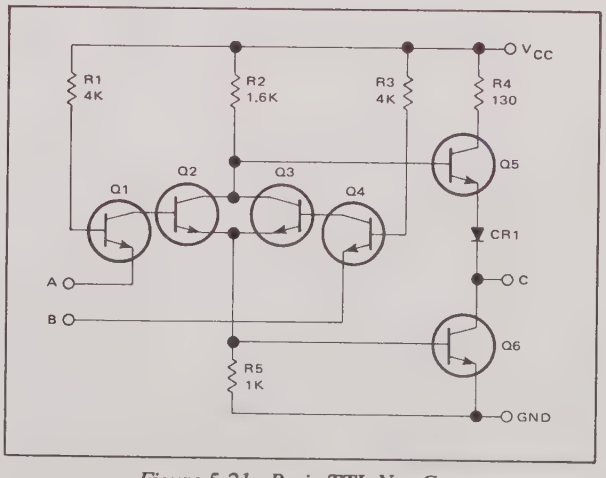


Figure 5.21 - Basic TTL Nor Gate

*E5 fb signal input
E6 fb signal low

5.98 The Nor gate is comprised of six transistors. The two input transistors, Q1 and Q4, are used as diode or gates (figure 5.22). Transistors Q2 and Q3 are voltage phase inverters. Transistors Q5 and Q6 form a totem-pole output. The totem-pole circuit has a low output resistance for both a high and low level.

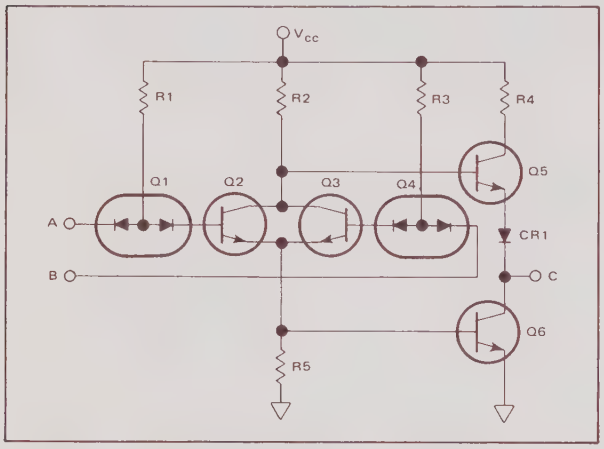


Figure 5.22 - Equivalent Circuit

5.99 Assume a Logical "0" level exists at both A and B inputs. Transistor Q1 and Q4 are conducting. Therefore, the collectors of Q1 and Q4 are at logical "0" level. The logical "0" level from the collectors of Q1 and Q4 are applied to the bases of Q2 and Q3 causing them to turn off. The collectors of Q2 and Q3 are connected together and to the base of Q5. The logical "1" on the base of Q5 causes Q5 to conduct. Output C is connected to the emitter of Q5 via CR1. Diode CR1 prevents an indeterminate output. The output of the Nor gate is two diode drops (1.4V) lower than the base voltages of Q5 or 3.6V.

5.100 Assume a logical "1" level is applied to input A. Base current for Q2 is supplied through R1 and the base-collector junction of Q1. Transistor Q2 is turned on. The collector of Q2 is connected to the base of Q5 and turns Q5 off. The emitter of Q2 is connected to the base of Q6. Q2 supplies base current to Q6 base; therefore Q6 is turned on and output C is low.

5.101 A logical "1" level applied to either or both inputs A or B result in a logical "0" level at output C. The truth table is shown in table 5.7.

5.102 Emitter Coupled Logic (ECL).

5.103 BASIC NOR FUNCTION.

5.104 A number of ECL integrated circuits are used in the counter. ECL circuits are used wherever high-speed switching is required. The basic Nor function is shown in figure 5.23. Logic levels used are:

Table 5.7 - Truth Table

A	B	C
1	1	0
1	0	0
0	1	0
0	0	1

Logical 0: 3.5V Logical 1: 4.2V

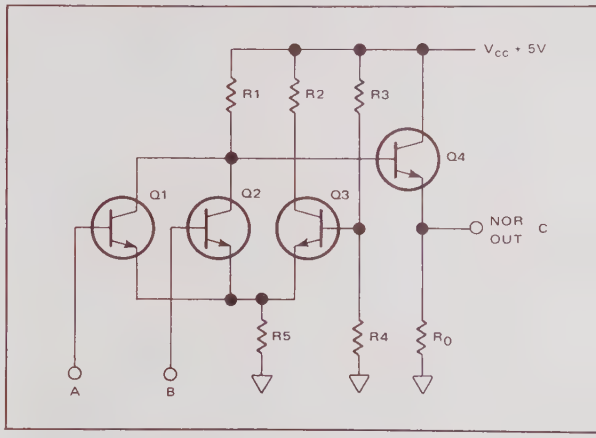


Figure 5.23 - Basic ECL Nor Gate

5.105 The gate is comprised of differential amplifier Q2 and Q3, input transistors Q1 and Q2, and emitter follower output transistor Q4. Transistor Q3 and resistors R3 and R4 form a fixed bias circuit.

5.106 Assume Logical "0" levels exist at both A and B inputs. Transistors Q1 and Q2 are cut off; therefore, the collectors of Q1 and Q2 are at a logical "1" level. The logical "1" level from the collectors of Q1 and Q2 is applied to the base of Q4, causing Q4 to conduct. The output at the emitter of Q4 is a logical "1" level (output C).

5.107 Assume that a logical "1" level is applied to input A. Transistor Q1 conducts and a logical "0" level results at the Q1 collector due to the drop across R1. The logical "0" level is applied to the base of Q4 causing Q4 to cut off providing a logical "0" level at output C.

5.108 A logical "1" level applied to either or both input A or B results in a logical "0" level at output C. The circuit therefore performs a Nor function; the truth table is shown in table 5.8.

Table 5.8 - ECL NOR Truth Table

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

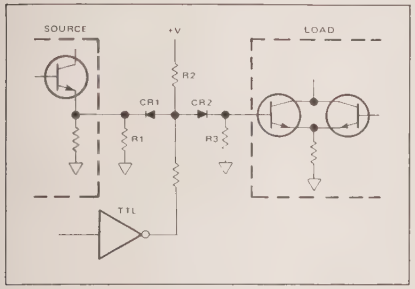


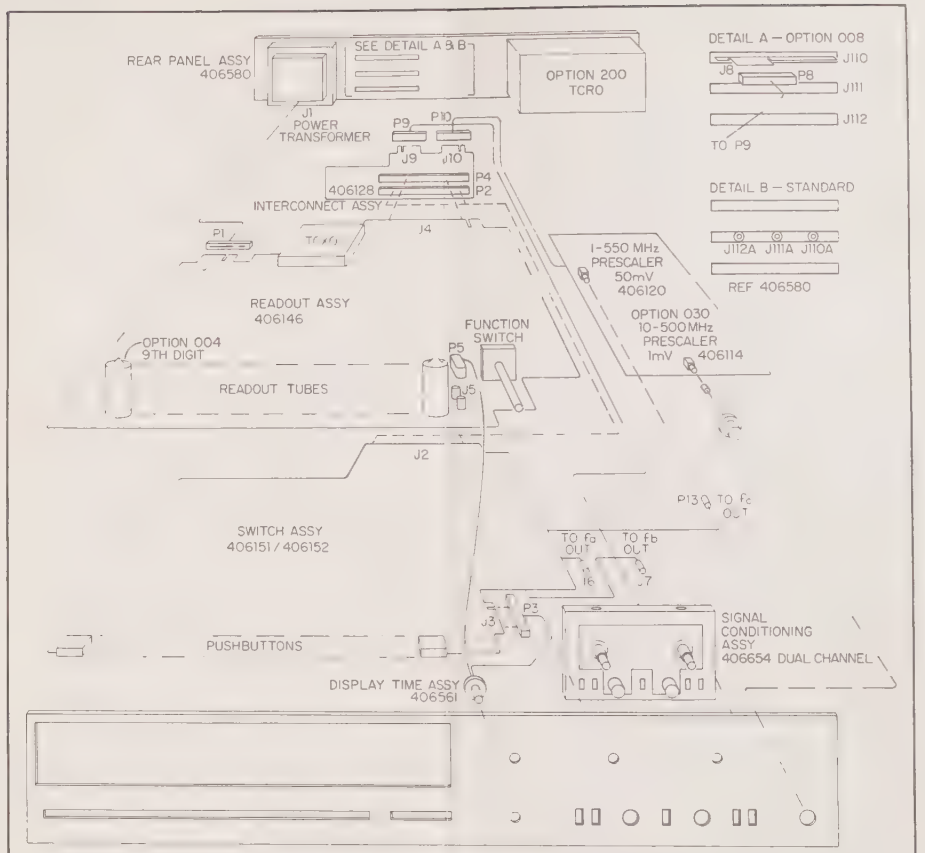
Figure 5.24 - Diode Gate

5.109 DIODE GATE.

5.110 The purpose of a diode gate (figure 5.24) is to control a ECL level signal with a TTL gate. The diode gate is much faster than TTL logic and speed is required in these circuits. Diode CR2 is always in forward conduction with the current provided through resistor R2 from V. The state of CR1 depends on the output of TTL gate. If the TTL gate is high, the CR1 conducts. If the TTL gate is low, then CR1 is reverse-biased and the signal is not transferred from the source to the load. If the output of the TTL gate and CR1 is forward biased, a low insertion loss signal path is provided between the source and the load. DC levels are maintained between the source and load as shown in table 5.9 due to CR1 and CR2 being connected back-to-back.

Table 5.9 - DC Levels

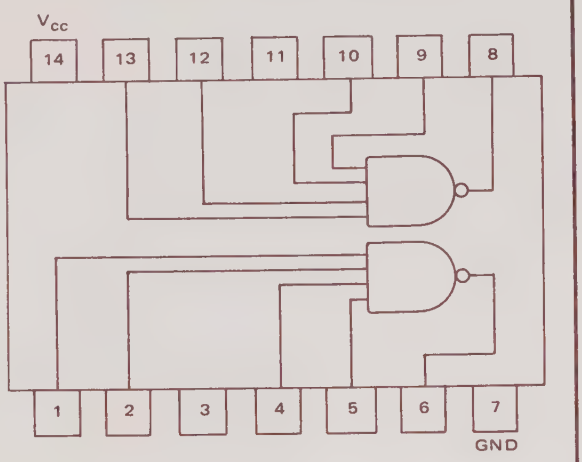
	TTL Gate High		TTL Gate Low	
V Source Output	3.4	4.2	3.4	4.2
V Load Input	3.4	4.2	3.14	3.14



ASSEMBLY NAME	MODEL	
	8015B	8035B
SIGNAL CONDITIONING	406654	406654
SWITCH BOARD	406151	406152
READOUT BOARD	406146	406146
REAR PANEL	406580	406580
550 MHz PRESCALER	NOTE ONLY 1 PRESCALER PER COUNTER	406120
500 MHz PRESCALER OPTION 030		406114
DISPLAY TIME CONTROL	406561	406561
INTERCONNECT BOARD	406128	406128
FRONT PANEL	730553	730556

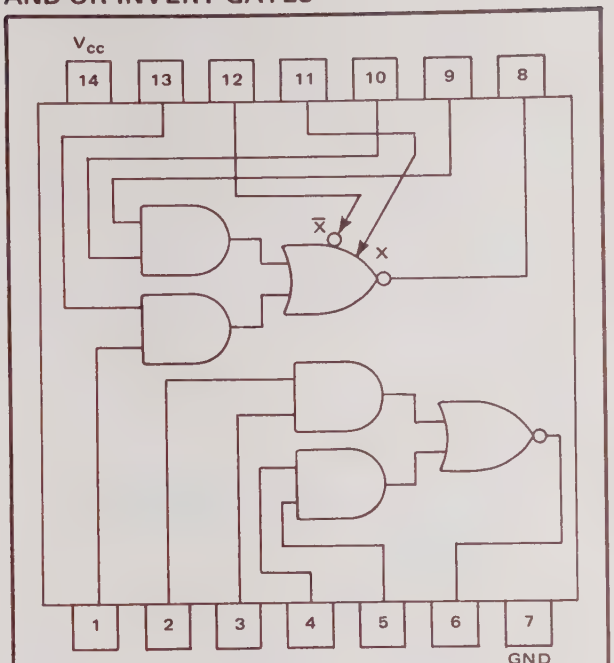
Figure 5.25 - Exploded View

7420
DUAL 4-INPUT POSITIVE NAND GATE

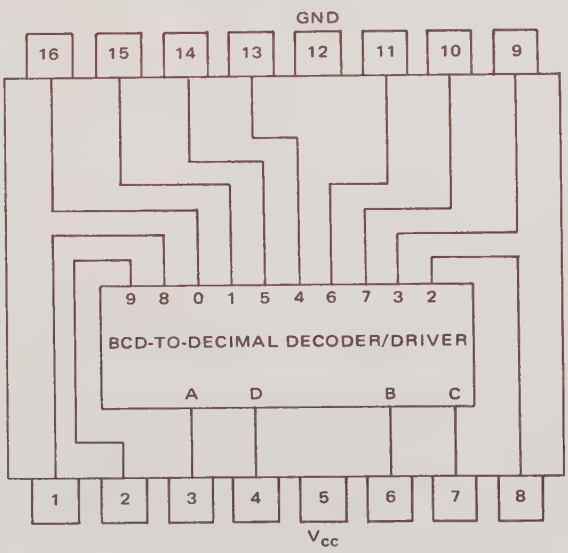


A	B	C	D	E
1	1	1	1	0
1	1	1	0	1
1	1	0	0	1
1	0	0	0	1
0	0	0	0	1

7451
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES



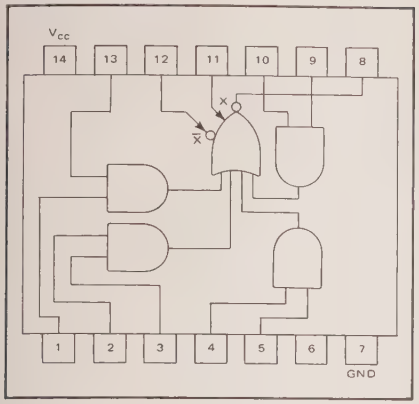
7441
BCD-TO-DECIMAL DECODER/DRIVER



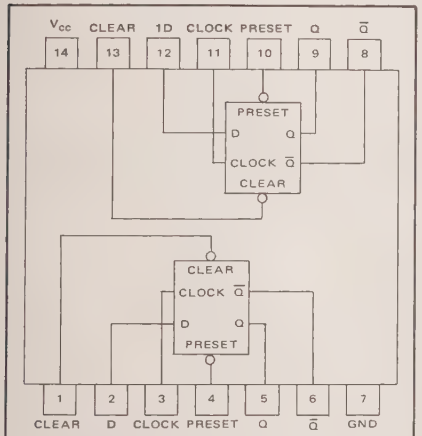
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Figure 5.26 - Integrated Circuits

7454
4-WIDE 2-INPUT AND-OR-INVERT GATE



74H74
DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP

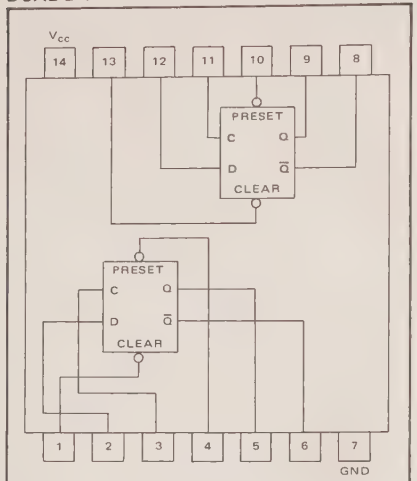


(Each Flip-Flop)		
t_n	t_{n+1}	
Input	Output	Output
D	Q	Q̄
L	L	H
H	H	L

H = High Level, L = Low Level

NOTES:
1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

7474
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



D_n	Q_{n+1}	$\bar{Q}_{n+1}$
1	1	0
0	0	1

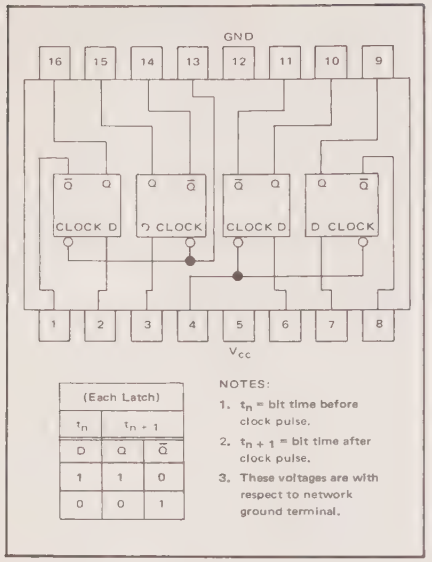
Preset	Clear	Q
1	1	Q
1	0	0
0	1	1
0	0	†

† Both outputs in 1 state

n is time prior to clock

n + 1 is time following clock

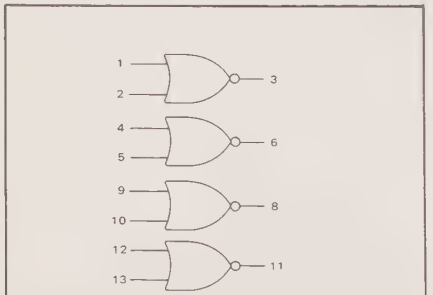
7475
QUADRUPLE BISTABLE LATCH



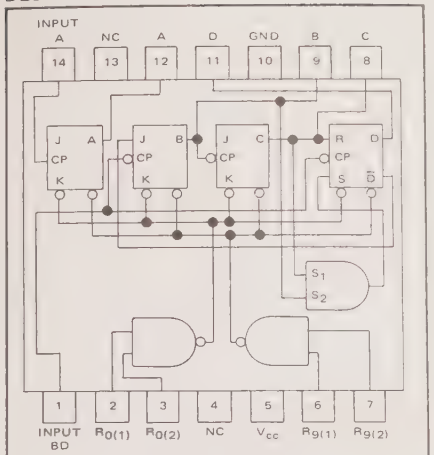
(Each Latch)		
t_n	t_{n+1}	
D	Q	Q̄
1	1	0
0	0	1

NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. These voltages are with respect to network ground terminal.

MC1010
QUAD 2-INPUT GATES



7490
DECADE COUNTER



BCD COUNT SEQUENCE (See Note 1)

	OUTPUT			
COUNT	D	C	B	A
0	0	0	0	0
1	0	0	0	0
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

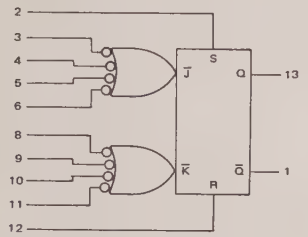
RESET/COUNT (See Note 2)

RESET INPUTS				OUTPUT			
$R_{0(2)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

NOTES:
1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 of a logical 0 may be present.
3. Fanout from output A to input BD and to 10 additional Series 54/74 loads is permitted.

Figure 5.26 - Integrated Circuits continued

MC1013/MC1027
AC-COUPLED J-K FLIP-FLOP



MC1013
DC Input Loading Factor = 1
DC Output Loading Factor = 25
tpd = 6.0 ns typ
Power Dissipation = 125 mW typ

MC1027
DC Input Loading Factor = 2
DC Output Loading Factor = 25
tpd = 4.0 ns typ
Power Dissipation = 250 mW typ

R-S TRUTH TABLE

Pin No.	R 12	S 2	Q^{n+1} 13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\overline{J}$-$\overline{K}$ inputs are static.
N.D. = Not defined.

$\overline{J}_D \cdot \overline{K}_D$ TRUTH TABLE

Pin No.	$\overline{J}_D$ *	$\overline{K}_D$ *	Q^{n+1} 13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

All other $\overline{J}$-$\overline{K}$ inputs and the R-S inputs are at a "0" level.

CLOCKED $\overline{J}$-$\overline{K}$ TRUTH TABLE

Pin No.	$\overline{J}$ *	$\overline{K}$ *	$\overline{C}_D$ **	Q^n 13
	Ø	Ø	0	Q^n
	0	0	1	$\overline{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

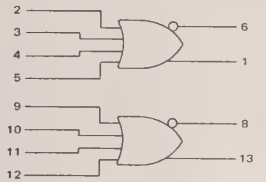
All other $\overline{J}$-$\overline{K}$ inputs and the R-S inputs are at a "0" level.
Ø = Either state will result in the desired output.

* Any $\overline{J}$ or $\overline{K}$ input, not used for $\overline{C}_D$.

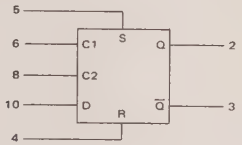
** $\overline{C}_D$ obtained by connecting one $\overline{J}$ and one $\overline{K}$ input together.

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} − 0.6V). Clock $\overline{C}_D$ is obtained by tying one $\overline{J}$ and one $\overline{K}$ input together.

MC1023
DUAL 4-INPUT CLOCK DRIVER



MC1034
TYPE D FLIP-FLOP



DC Input Loading Factor:
C = 1, D = 2, R and S = 6
DC Output Loading Factor = 25
Power Dissipation = 185 mW typical using external 600-ohm pull-down resistors
240 mW typical using internal pull-down resistors

R-S TRUTH TABLE

Pin No.	R 4	S 5	Q^{n+1} 2	$\overline{Q}^{n+1}$ 3
	0	0	Q^n	$\overline{Q}^n$
	0	1	1	0
	1	0	0	1
	1	1	N.D.	N.D.

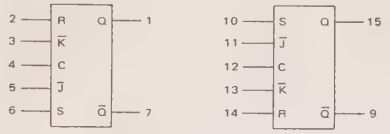
N.D. = Not Defined

CLOCKED TRUTH TABLE

Pin No.	D 10	C 6 or 8	Q^{n+1} 2	$\overline{Q}^{n+1}$ 3
	0	0	Q^n	$\overline{Q}^n$
	1	0	Q^n	$\overline{Q}^n$
	0	1*	0	1
	1	1*	1	0

*A "1" or Clock input is defined for this flip-flop as a change in level from a low state to a high state of the clock.

MC1032
100-MHz AC-COUPLED DUAL J-K FLIP-FLOP



V_{CC} = Pin 16
V_{EE} = Pin 8

DC Input Loading Factor:
Clock = 2
$\overline{J}$, $\overline{K}$, S, R = 1
DC Output Loading Factor = 25
tpd = 4.5 ns typ
Power Dissipation = 180 mW typ

R-S TRUTH TABLE

Pin No.	R 2 & 14	S 6 & 10	Q^{n+1} 1 & 15
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\overline{J}$-$\overline{K}$ inputs and Clock inputs are static
N.D. = Not defined

$\overline{J}_D$-$\overline{K}_D$ TRUTH TABLE

Pin No.	$\overline{J}$ *	$\overline{K}$ *	Q^{n+1} 1 & 15
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

All Clock inputs and the R-S inputs are at a "0" level.

CLOCKED $\overline{J}$-$\overline{K}$ TRUTH TABLE

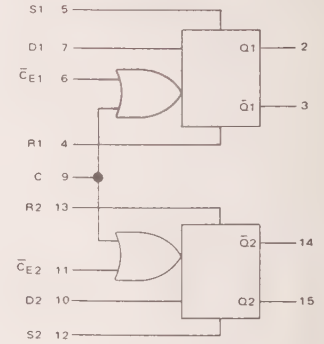
Pin No.	$\overline{J}$ *	$\overline{K}$ *	Clock 4 & 12	Q^n 1 & 15
	Ø	Ø	0	Q^n
	0	0	1	$\overline{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All other $\overline{J}$-$\overline{K}$ inputs and the R-S inputs are at a "0" level.
Ø = Either state will result in the desired output.

* Any $\overline{J}$ or $\overline{K}$ input

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the clock input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logic "1" only while the clock input is in a logic "1" state. (Clock maximum "1" level = V_{CC} − 0.7V.)

MC10131
DUAL TYPE D MASTER-SLAVE FLIP-FLOP



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

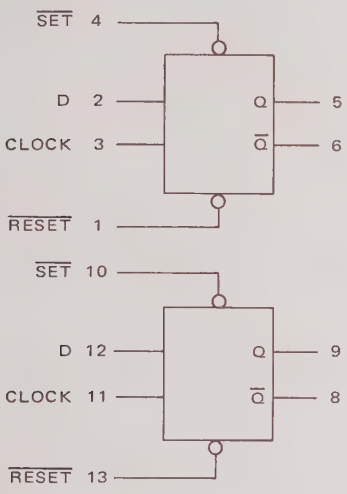
R-S TRUTH TABLE

R	S	Q^{n+1}	$\overline{Q}^{n+1}$
L	L	Q^n	$\overline{Q}^n$
L	H	H	L
H	L	L	H
H	H	N.D.	N.D.

N.D. = Not Defined

SEQUENTIAL TRUTH TABLE

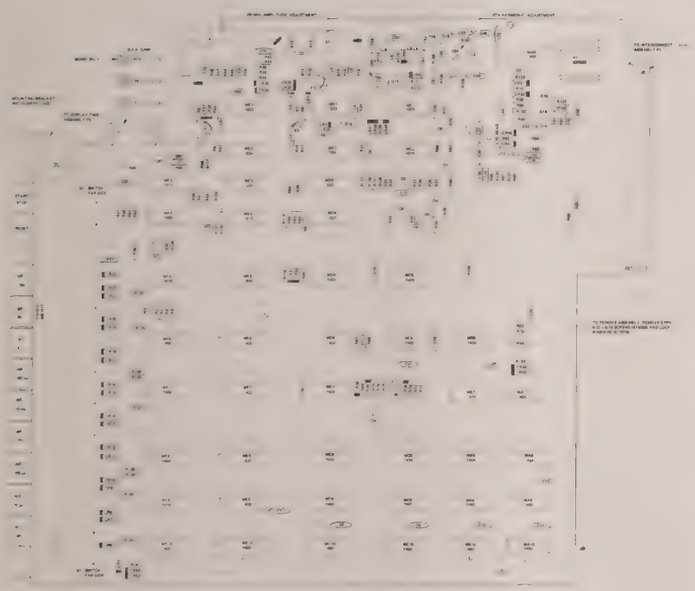
D	C	$\overline{C}_E$	Q_{n+1}
L	L	L	Q_n
L	L	H	L
L	H	L	Q_n
L	H	H	Q_n
H	L	L	Q_n
H	L	H	H
H	H	L	Q_n
H	H	H	Q_n

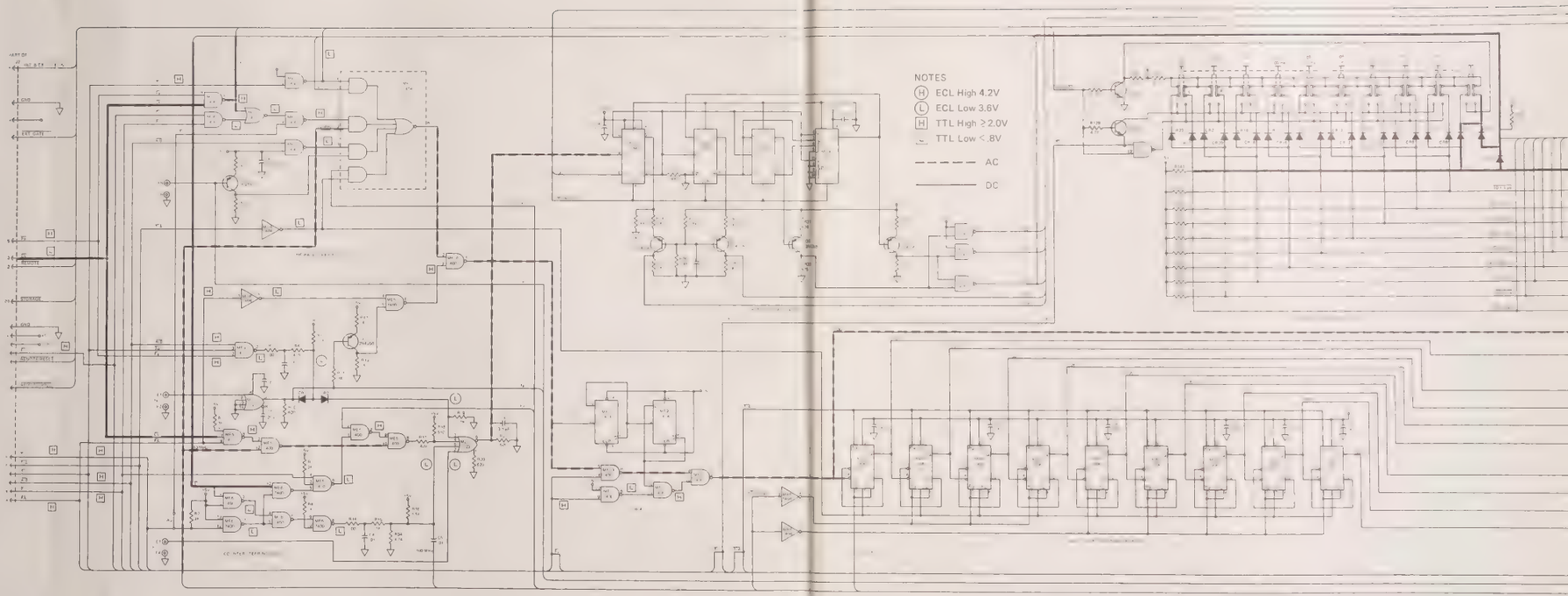


TRUTH TABLE

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$Q^{n+1} = D^n$





5-20 *Figure 5.27 - Signal Flow For Check Mode*

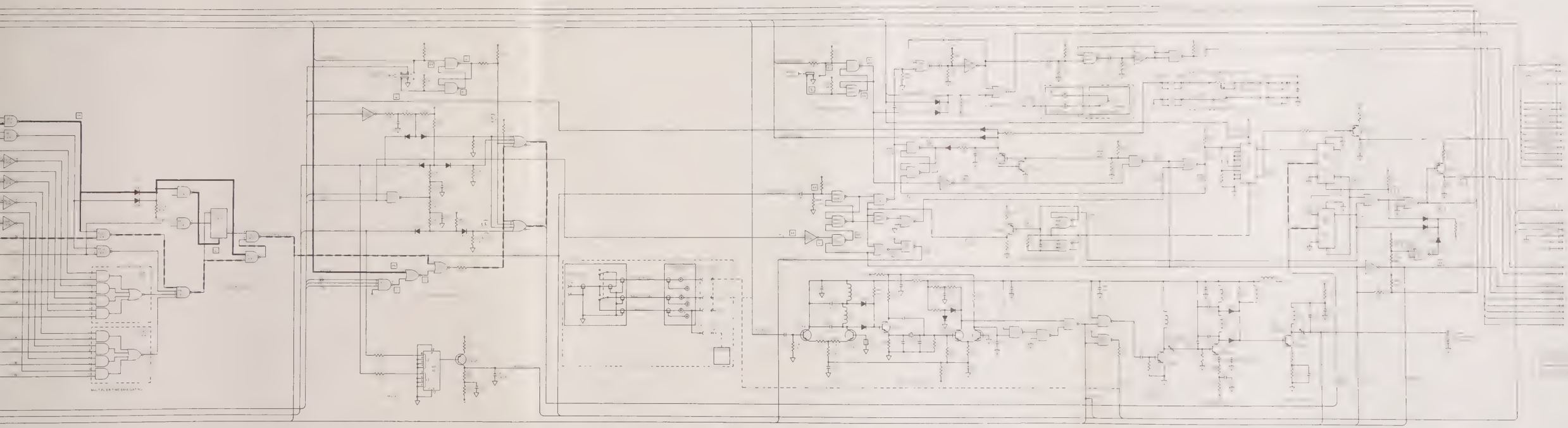
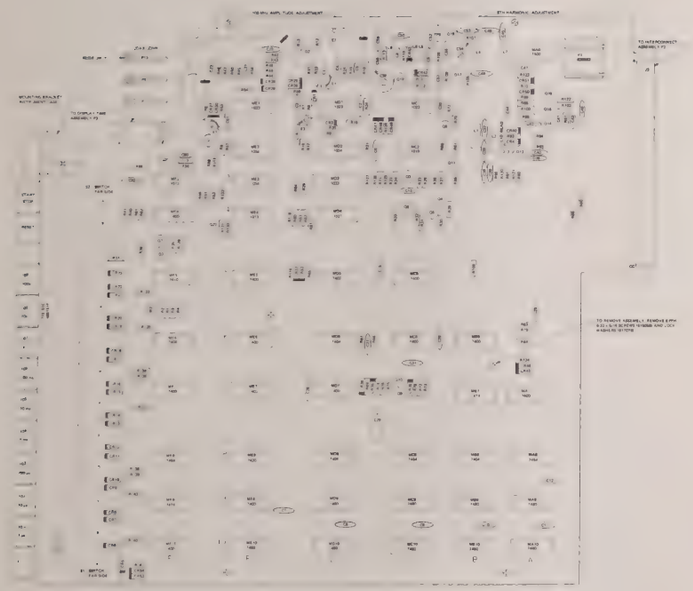
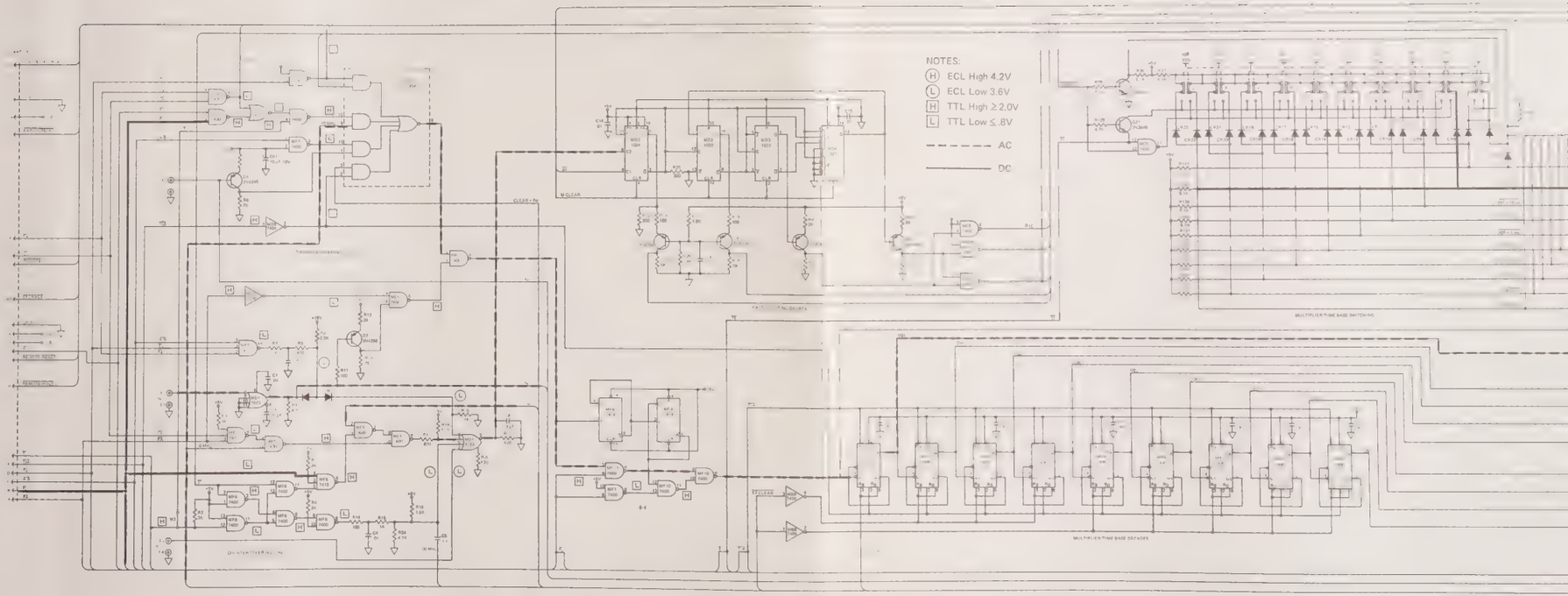
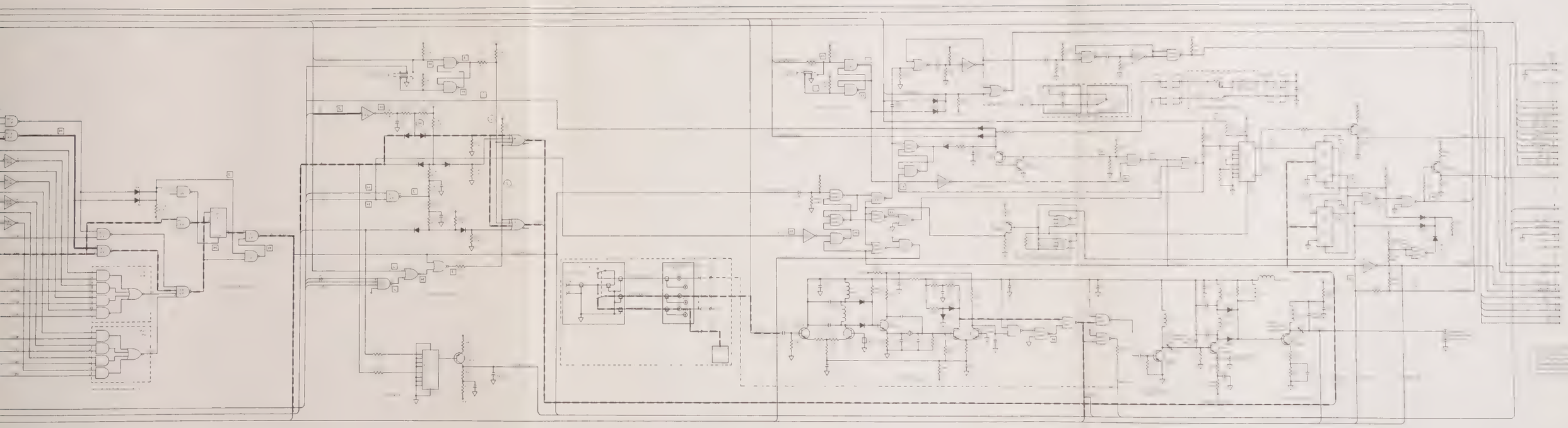


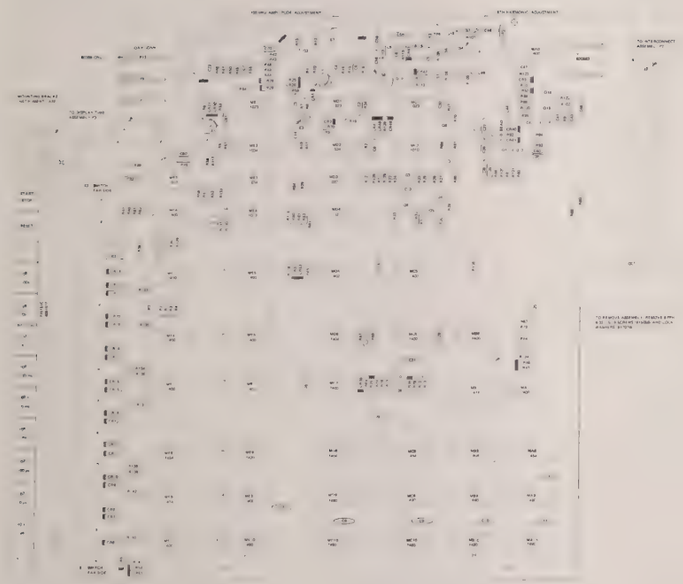
Figure 5.27 - Signal Flow For Check Mode 5-21

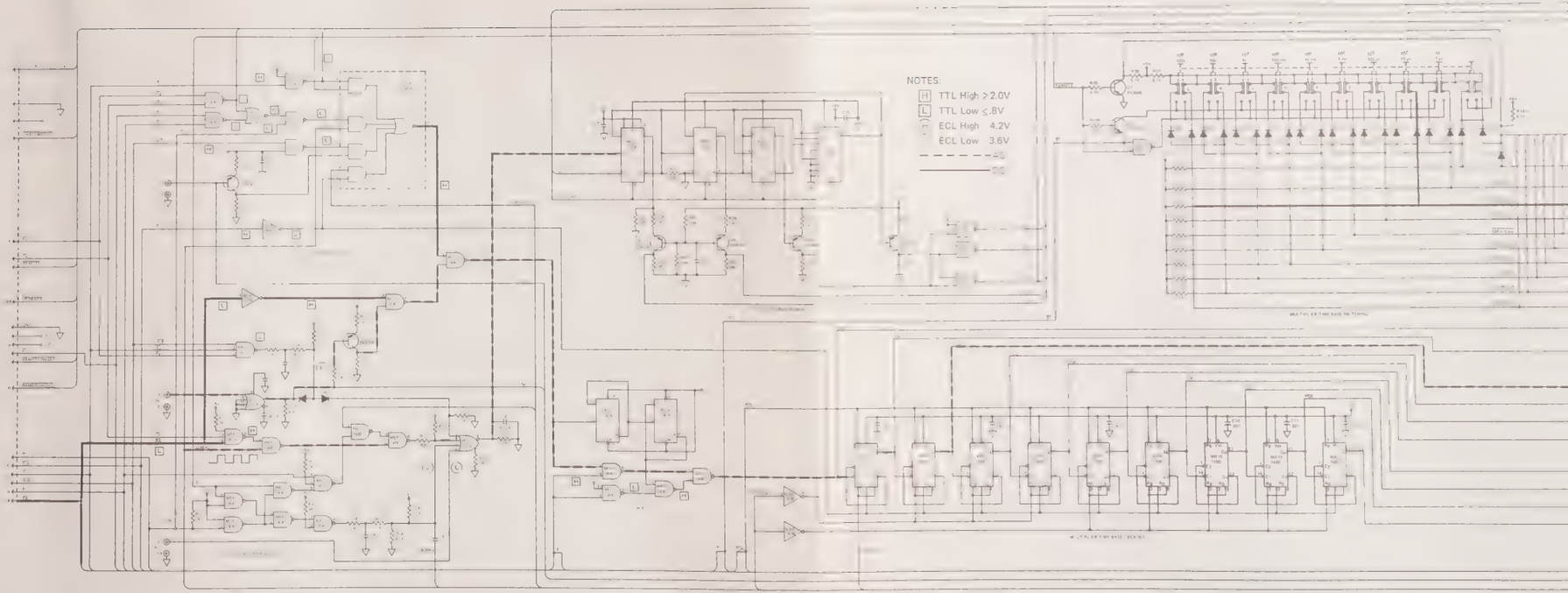




5-22 Figure 5.28 - Signal Flow For Period Mode






NOTES:
H TTL High ≥ 2.0V
L TTL Low ≤ .8V
ECL High 4.2V
ECL Low 3.6V

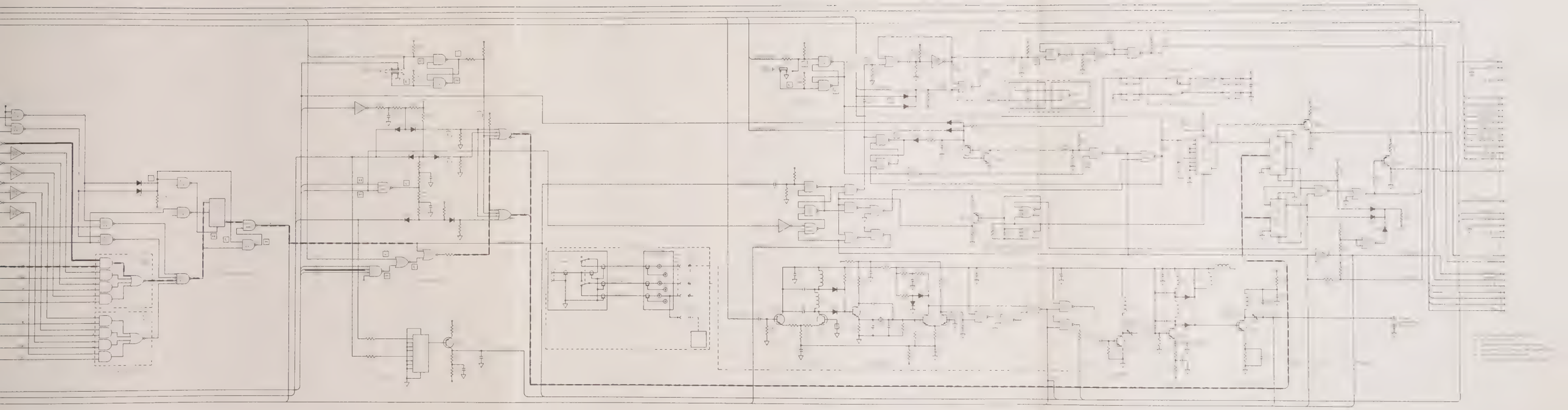
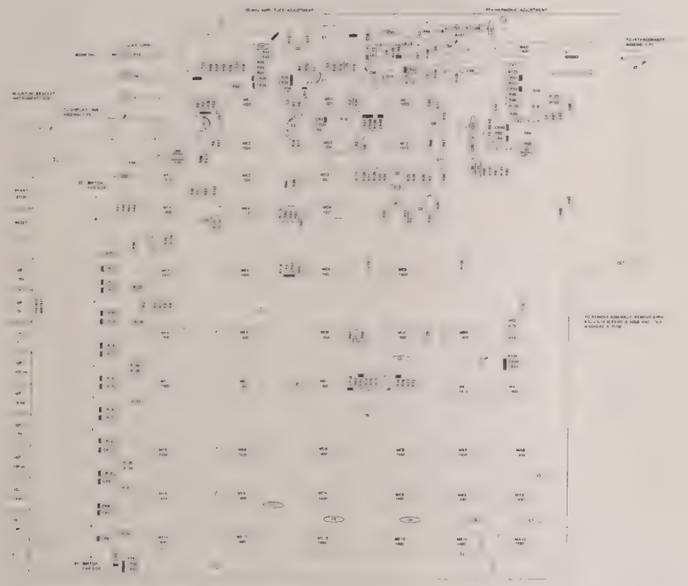
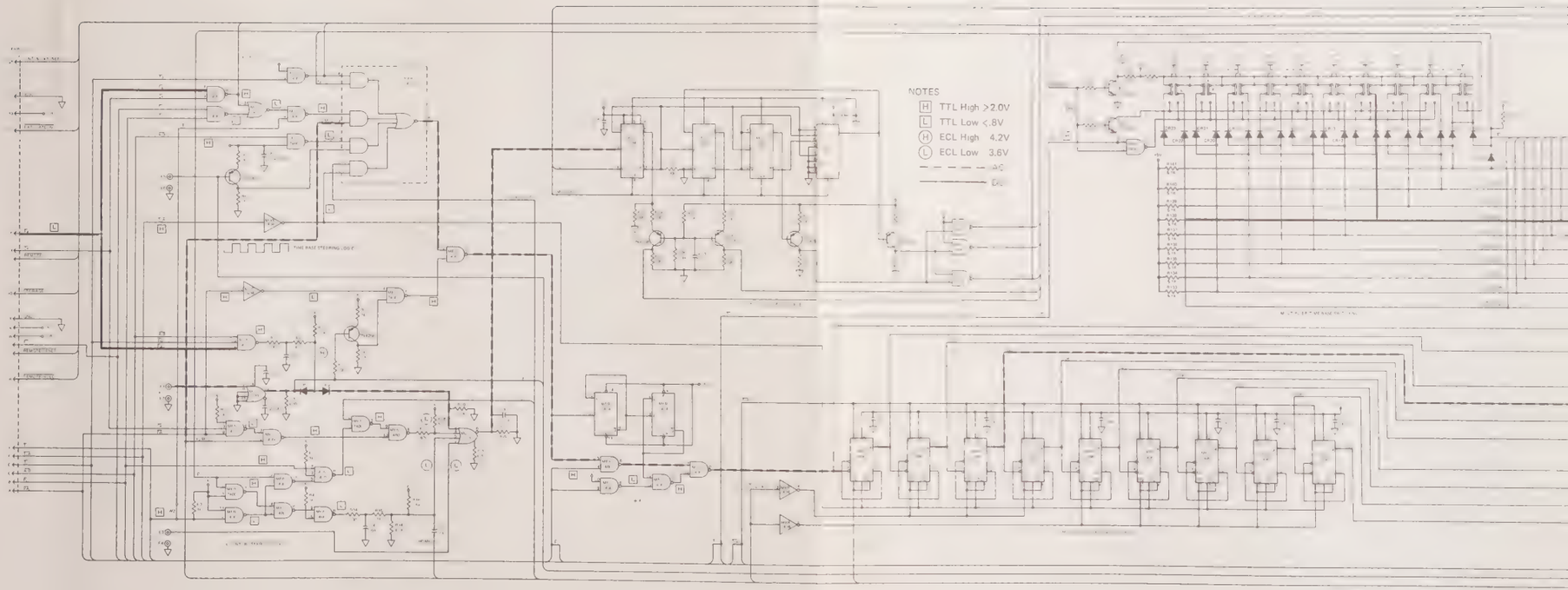


Figure 5.29 - Signal Flow For Period Average Mode





5-26 Figure 5.30 - Signal Flow For Frequency A Mode

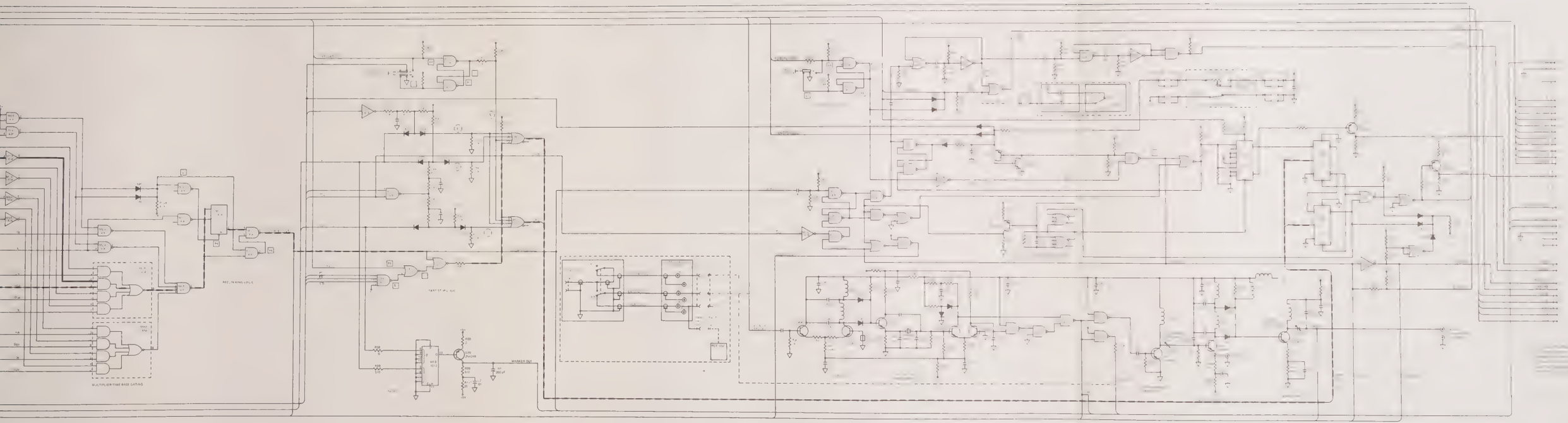
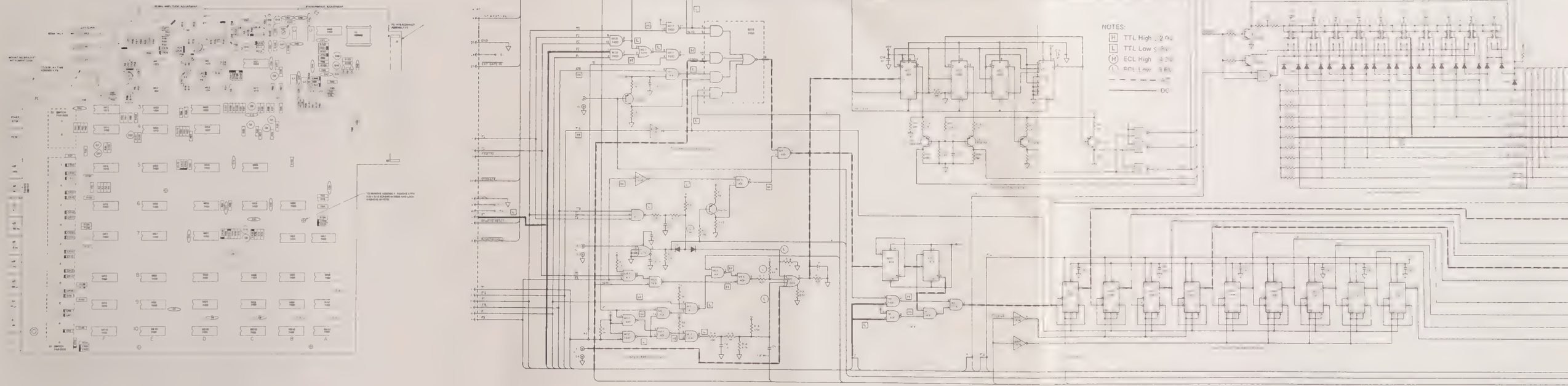


Figure 5.30 - Signal Flow For Frequency A Mode 5-27



5-28 Figure 5.31 - Signal Flow For Frequency C Mode

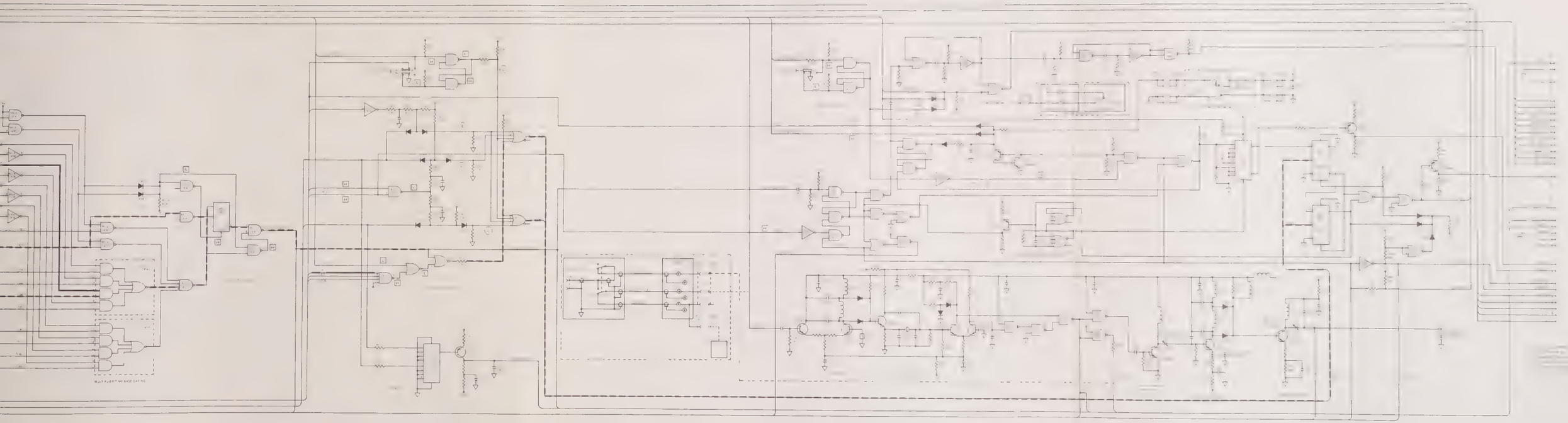
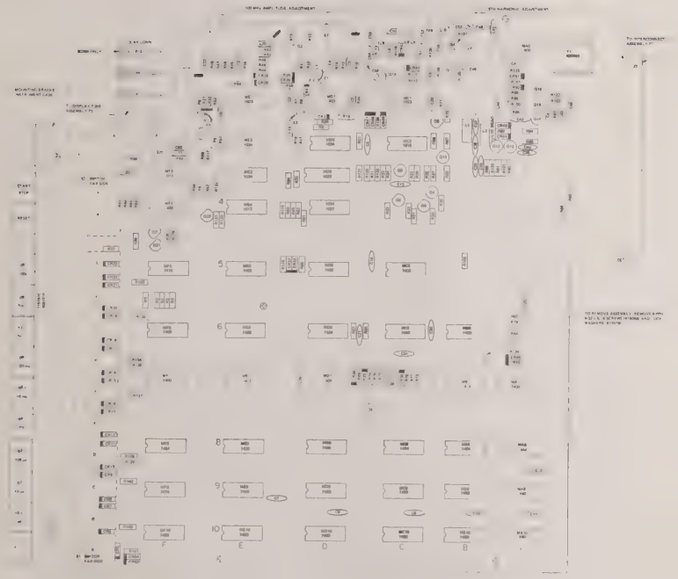
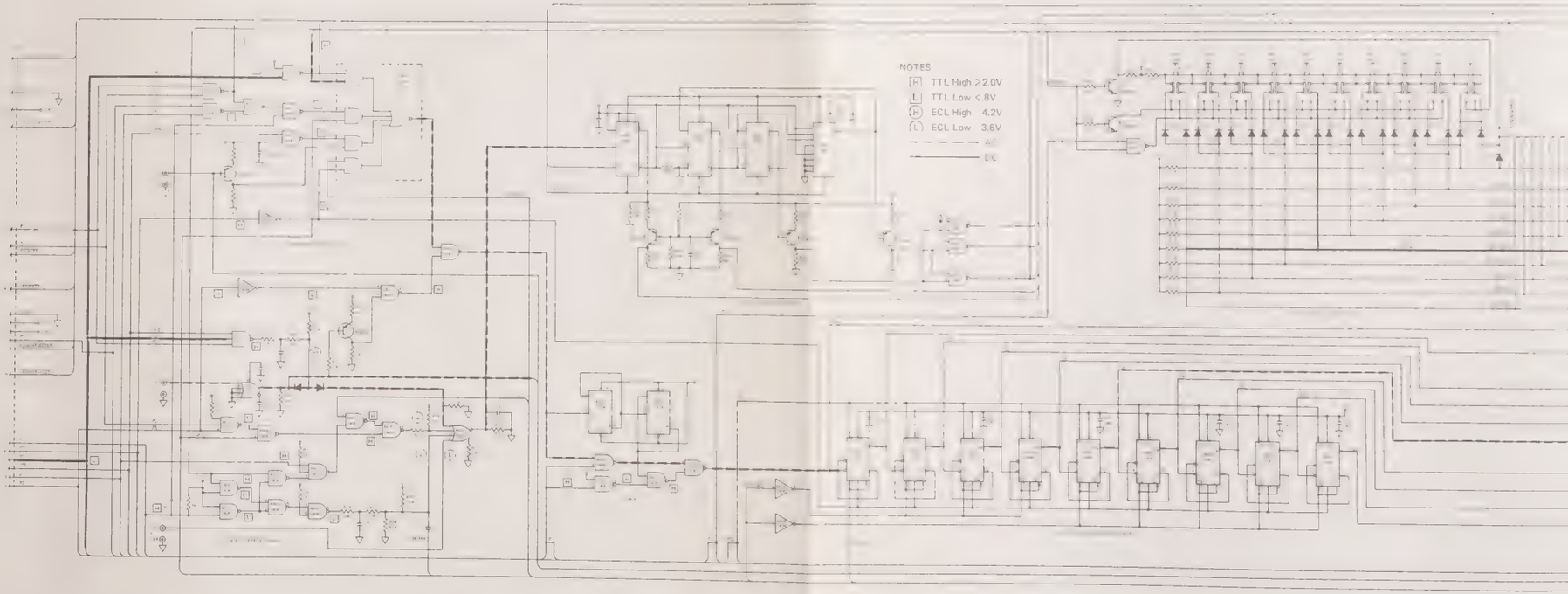


Figure 5.31 - Signal Flow For Frequency C Mode 5-29





5-30 *Figure 5.32 - Signal Flow For Totalize Mode*

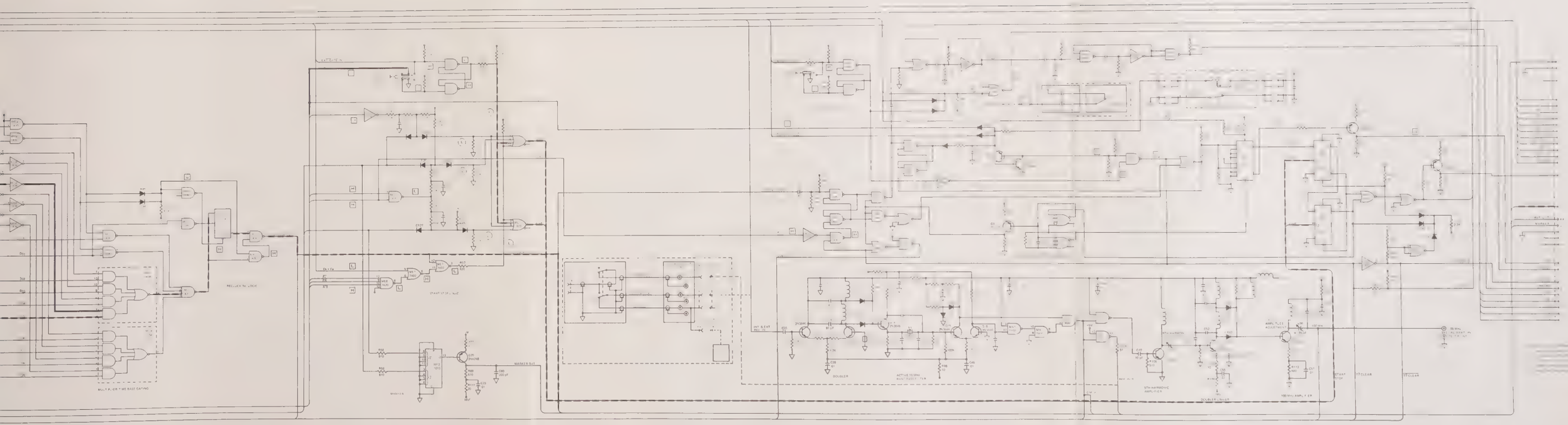
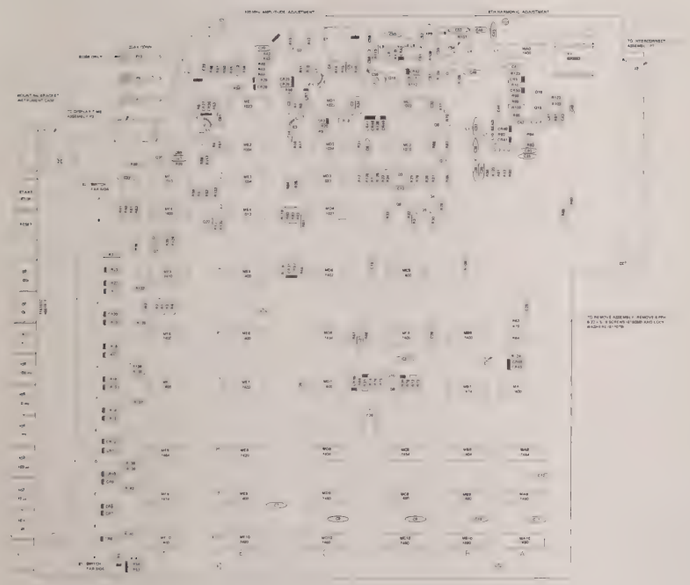


Figure 5.32 - Signal Flow For Totalize Mode



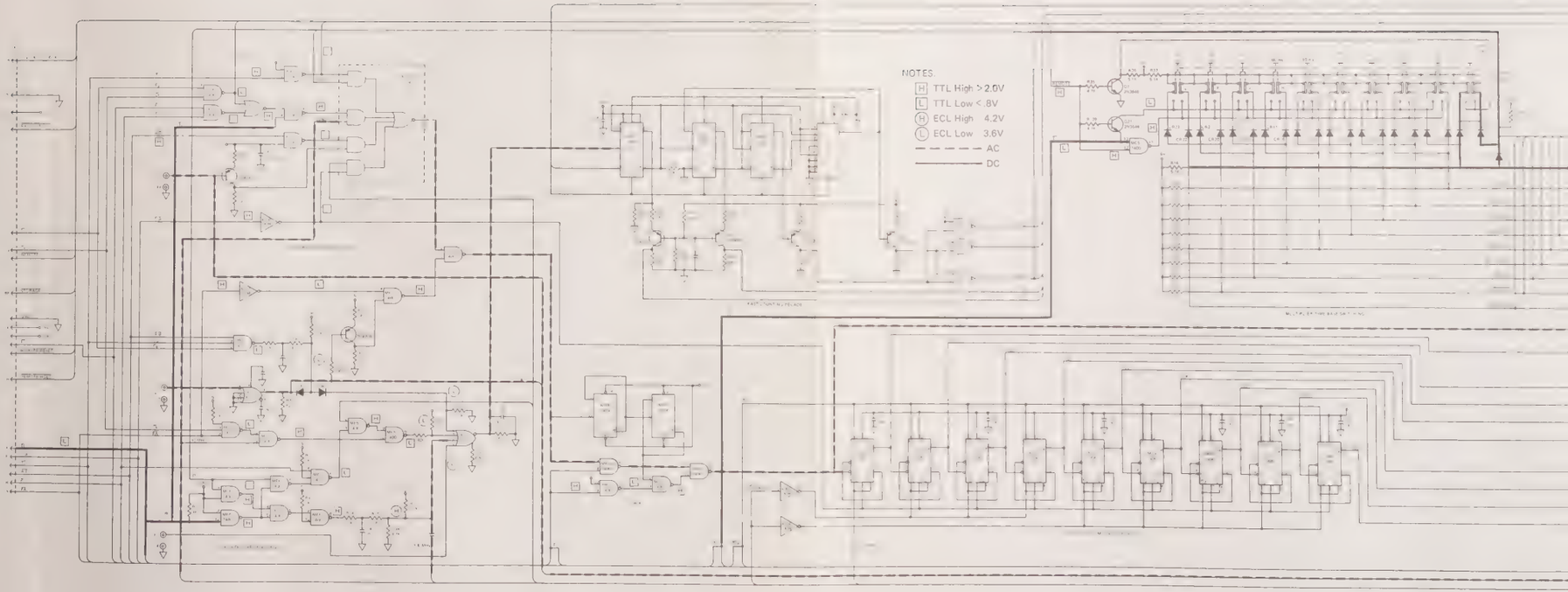


 Figure 5.33 - Signal Flow For Time Interval Mode

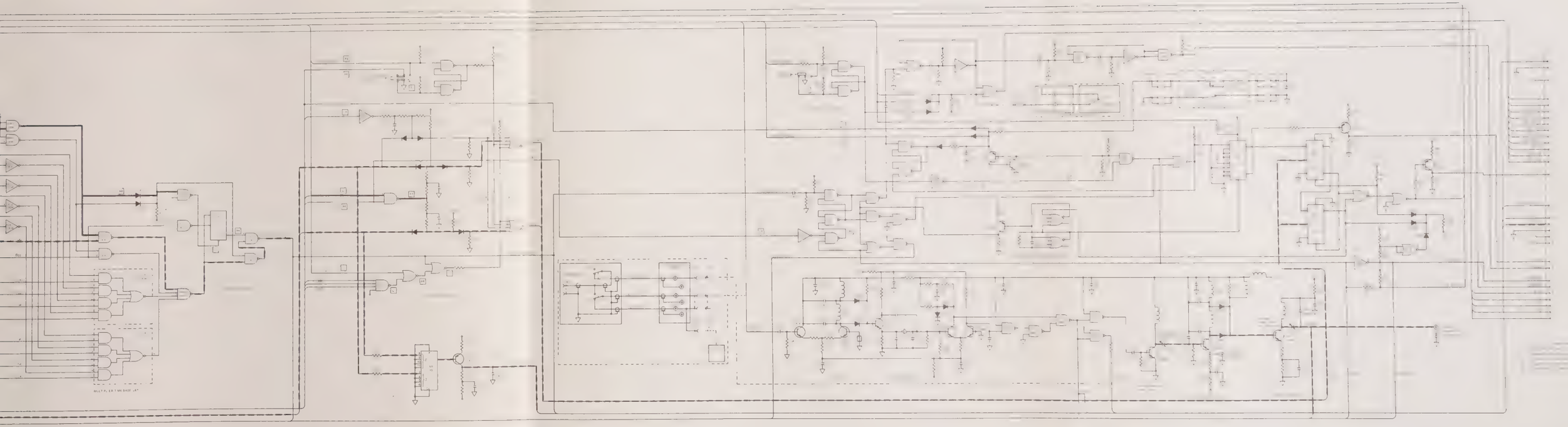
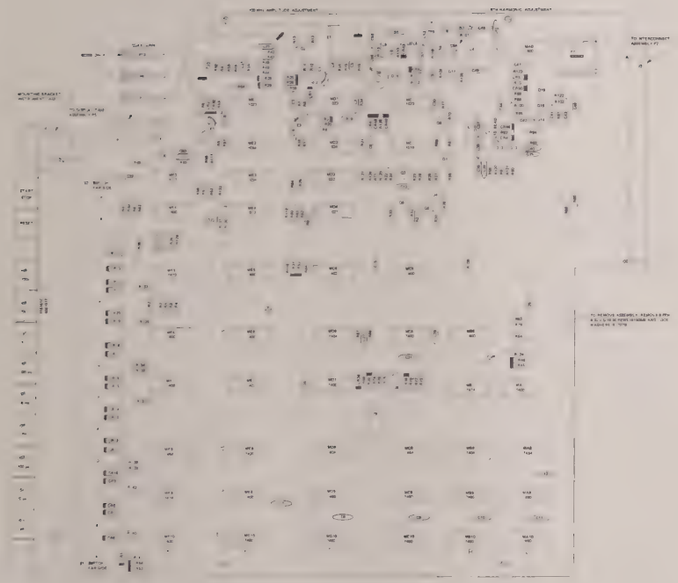
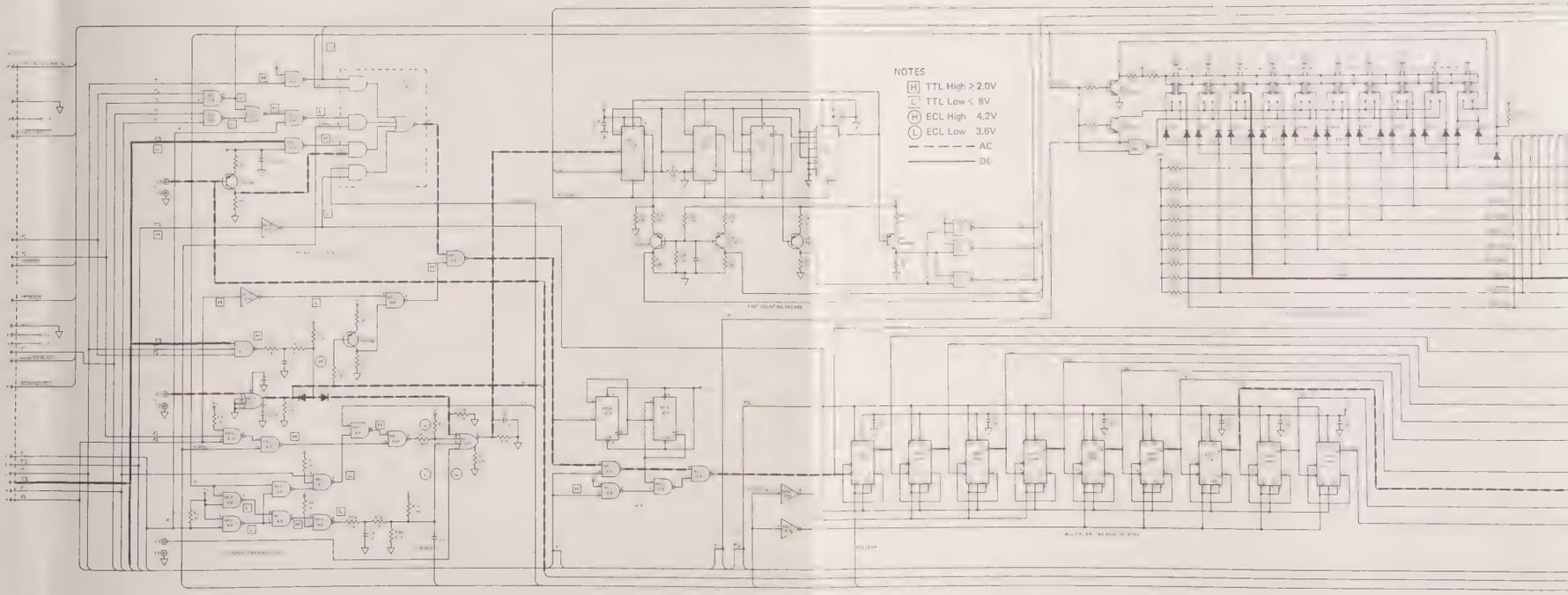


Figure 5.33 - Signal Flow For Time Interval Mode 5-33





5-34 Figure 5.34 - Signal Flow For Ratio Mode

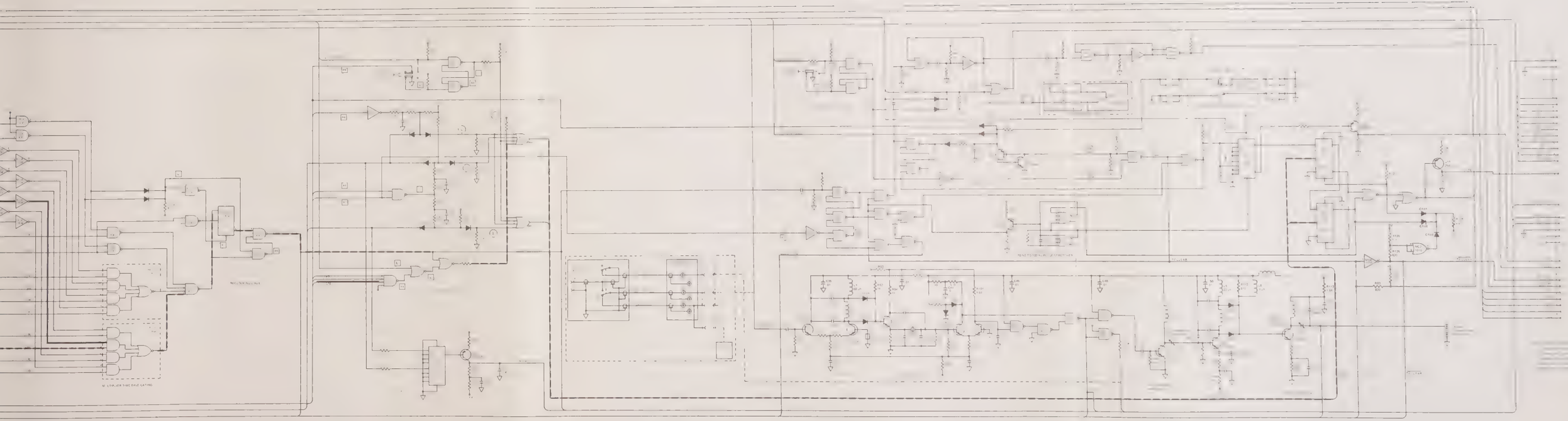


Figure 5.34 - Signal Flow For Ratio Mode

SECTION 6 SCHEMATICS

Figure	Title	Page
6.1	Layout, Signal Conditioning	6-2
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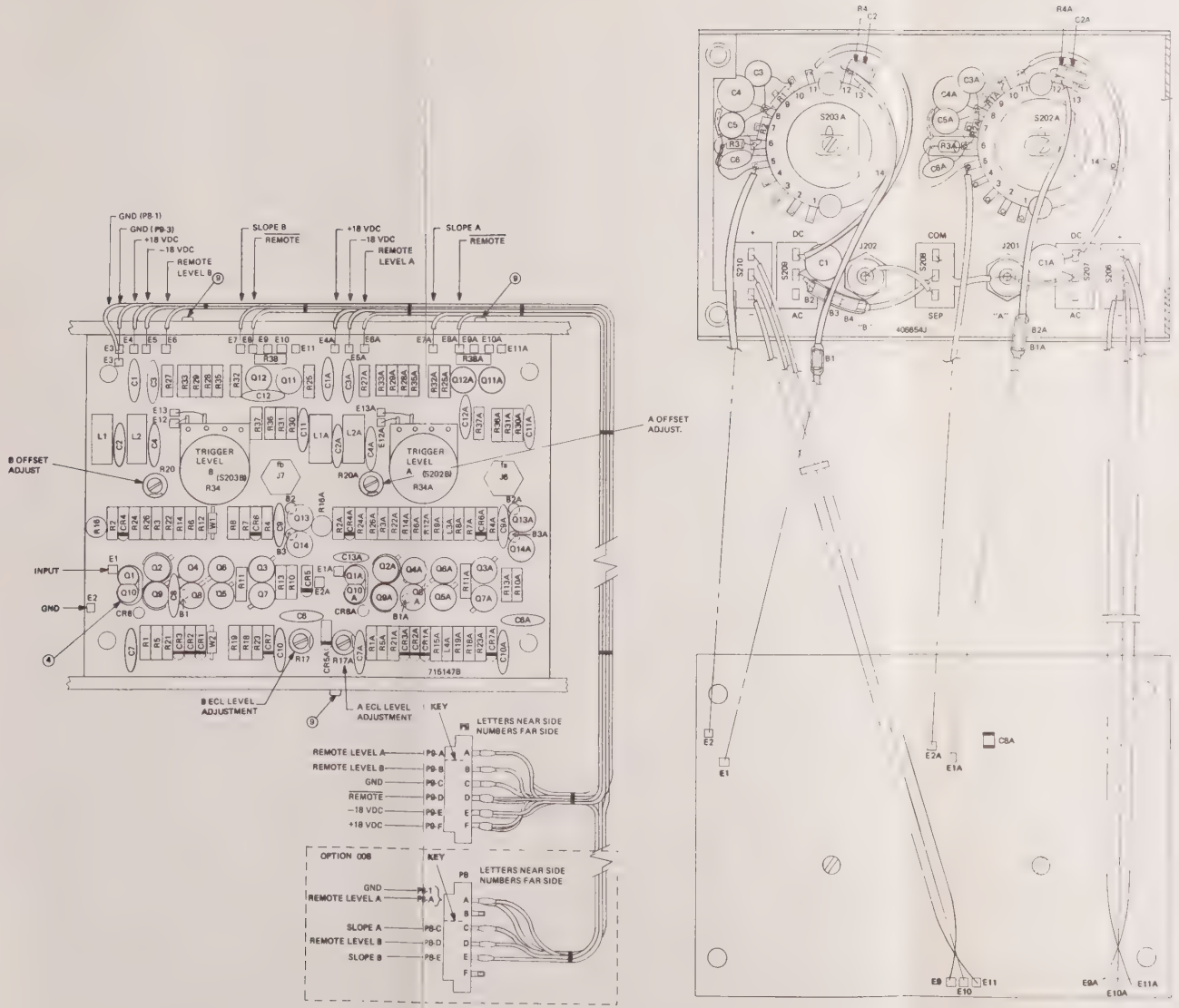
6.4	Schematic, Switch Board	6-5
6.5	Layout, Readout Board	6-6
6.6	Schematic, Readout Board	6-7
6.7	Schematic, Interconnect Board	6-8
6.8	Layout, Rear Panel	6-9
6.9	Schematic, Rear Panel	6-9
6.10	Layout, Systems Interface	6-11
6.11	Schematic, Systems Interface	6-11



6-2 Figure 6.1 - Layout, Signal Conditioning – Dual

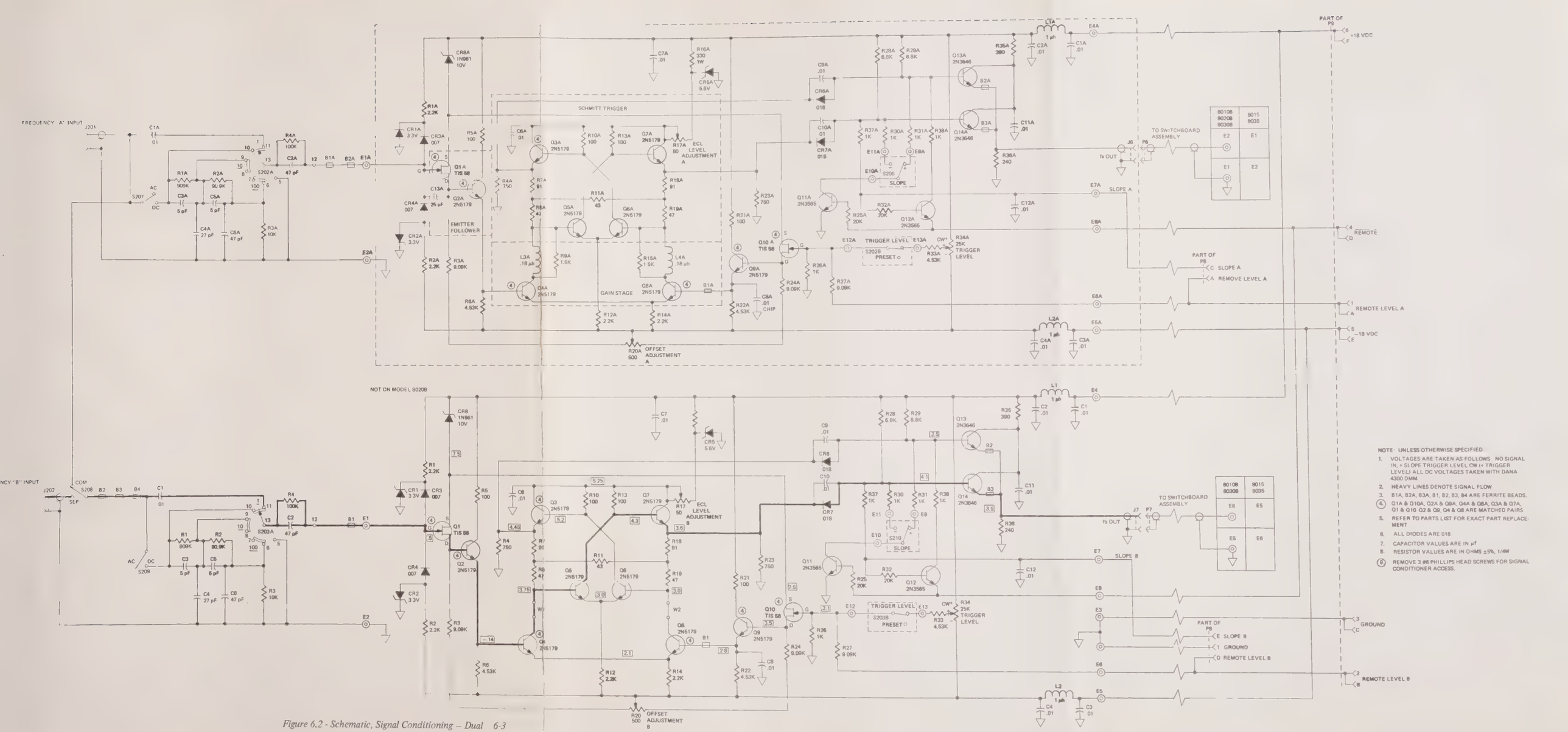
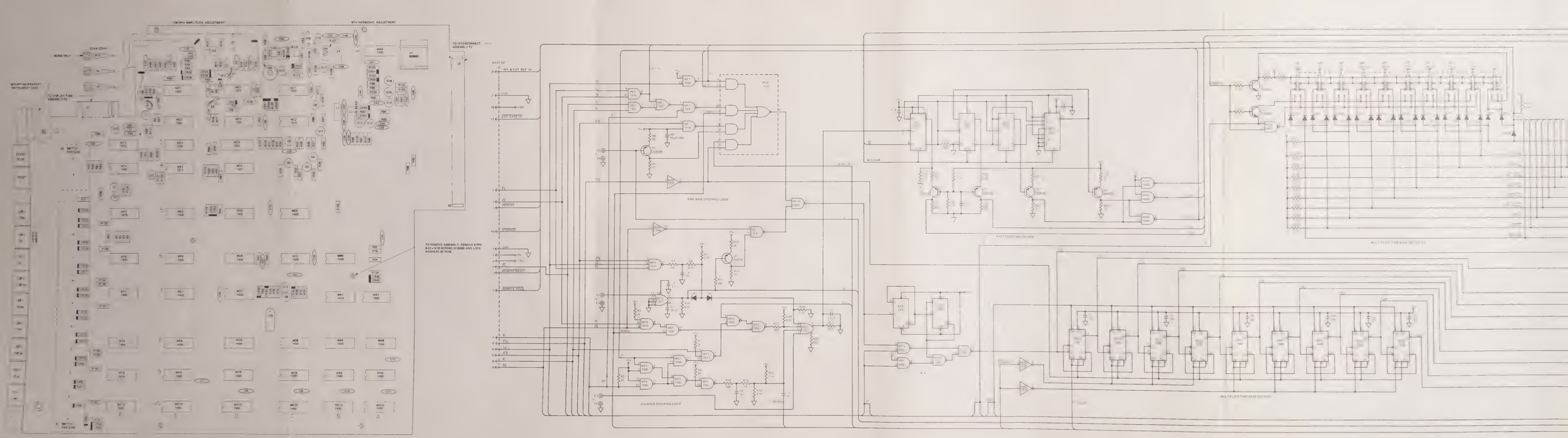

FREQUENCY "A" INPUT
J201
S207
AC
DC
S202A
SCHMITT TRIGGER
EMITTER FOLLOWER
GAIN STAGE
ECL LEVEL ADJUSTMENT A
TRIGGER LEVEL
PRESET
SLOPE
OFFSET ADJUSTMENT A
TO SWITCHBOARD ASSEMBLY
PART OF P9
+18 VDC
REMOTE
PART OF P8
C SLOPE A
A REMOVE LEVEL A
REMOTE LEVEL A
-18 VDC
NOT ON MODEL 80208
FREQUENCY "B" INPUT
J202
S208
S209
S203A
ECL LEVEL ADJUSTMENT B
S210
OFFSET ADJUSTMENT B
E SLOPE B
1 GROUND
D REMOTE LEVEL B
GROUND
REMOTE LEVEL B
80108 80208 80308
8015 8035
NOTE: UNLESS OTHERWISE SPECIFIED
1. VOLTAGES ARE TAKEN AS FOLLOWS: NO SIGNAL IN, + SLOPE TRIGGER LEVEL CW (+ TRIGGER LEVEL) ALL DC VOLTAGES TAKEN WITH DANA 4300 DMM.
2. HEAVY LINES DENOTE SIGNAL FLOW
3. B1A, B2A, B3A, B1, B2, B3, B4 ARE FERRITE BEADS.
4. Q1A & Q10A, Q2A & Q9A, Q4A & Q8A, Q3A & Q7A, Q1 & Q10, Q2 & Q9, Q4 & Q8 ARE MATCHED PAIRS
5. REFER TO PARTS LIST FOR EXACT PART REPLACEMENT
6. ALL DIODES ARE 018
7. CAPACITOR VALUES ARE IN µf
8. RESISTOR VALUES ARE IN OHMS ±5%, 1/4W
9. REMOVE 3 #6 PHILLIPS HEAD SCREWS FOR SIGNAL CONDITIONER ACCESS.

Figure 6.2 - Schematic, Signal Conditioning – Dual 6-3



6-4 *Figure 6-3 - Layout, Switch Board 10-NS*

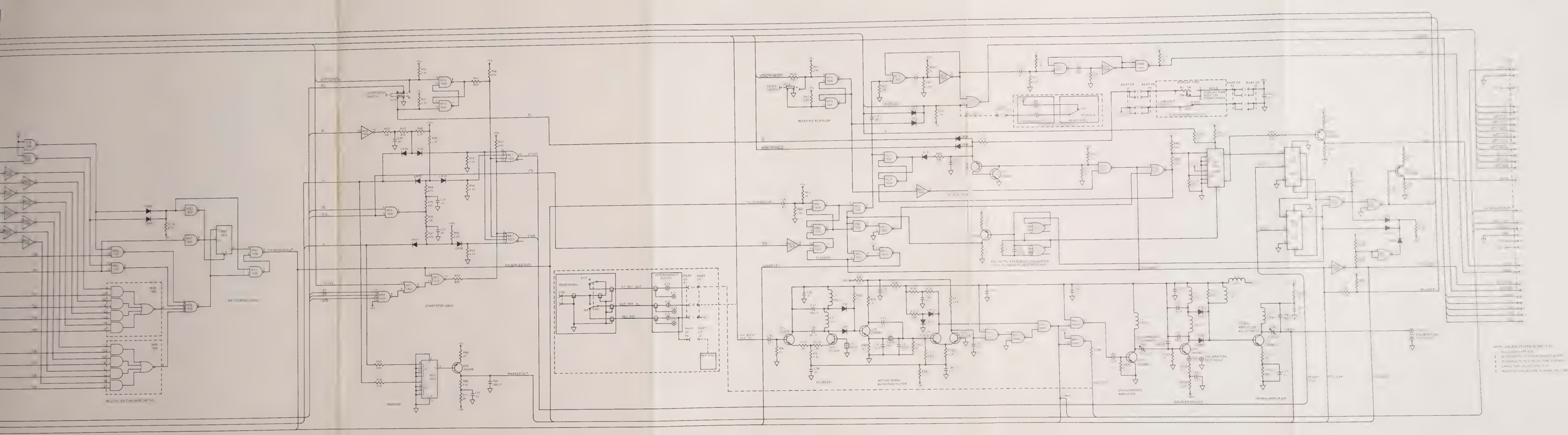


Figure 6.4 - Schematic, Switch Board 10 NS 6-5

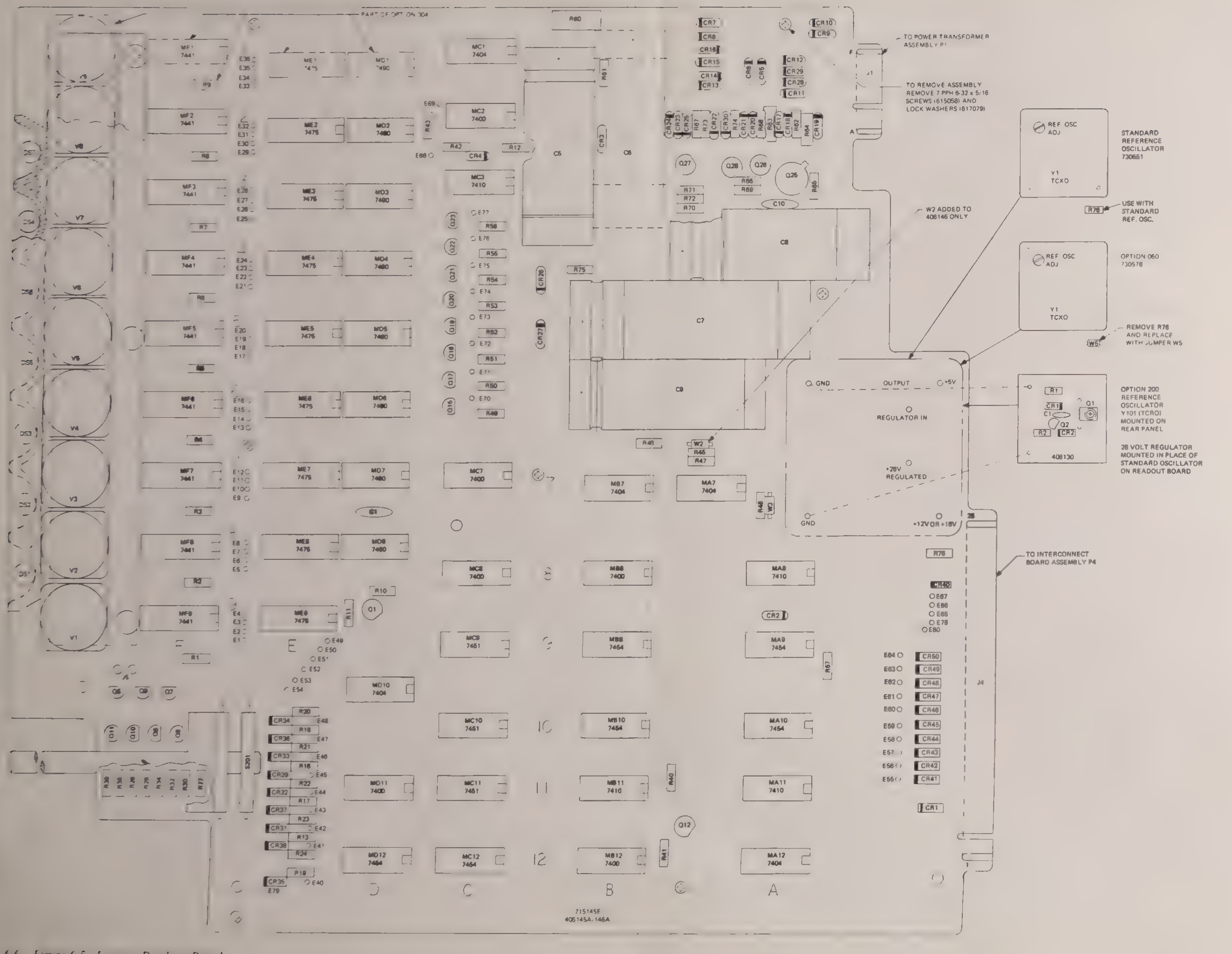
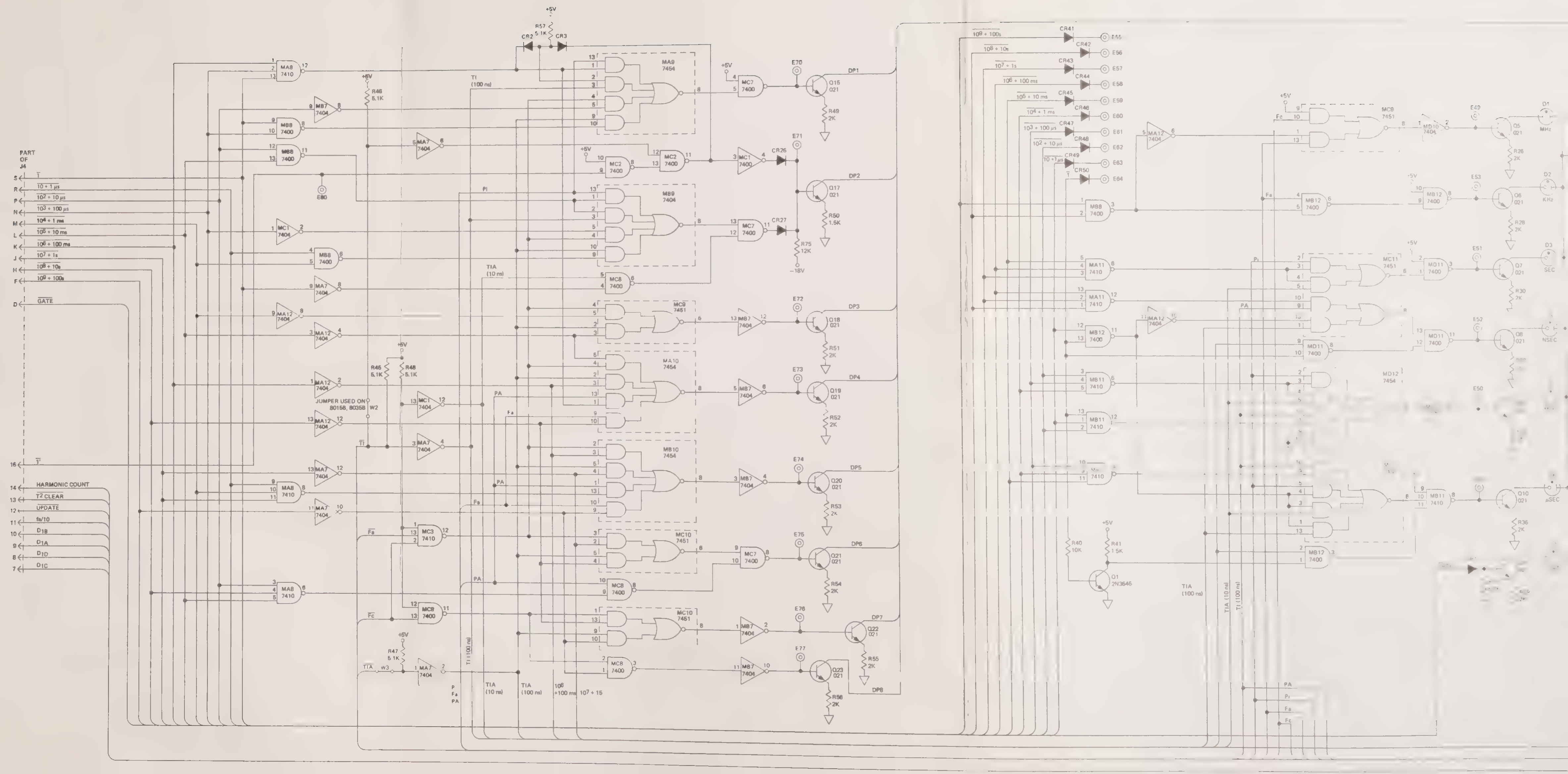

PART OF OPTION 004
TO POWER TRANSFORMER ASSEMBLY P1
TO REMOVE ASSEMBLY REMOVE 7 PPH 6-32 x 5/16 SCREWS (615058) AND LOCK WASHERS (617079)
STANDARD REFERENCE OSCILLATOR 730551
REF. OSC ADJ
Y1 TCXO
USE WITH STANDARD REF. OSC.
W2 ADDED TO 408146 ONLY
OPTION 060 730578
REMOVE R76 AND REPLACE WITH JUMPER W5
OPTION 200 REFERENCE OSCILLATOR Y101 (TCRO) MOUNTED ON REAR PANEL
28 VOLT REGULATOR MOUNTED IN PLACE OF STANDARD OSCILLATOR ON READOUT BOARD
408130
GND
OUTPUT
+5V
REGULATOR IN
+28V REGULATED
+12V OR +18V
TO INTERCONNECT BOARD ASSEMBLY P4
J4
715145E
408145A, 146A

 Figure 6.5 - Layout, Readout Board


PART OF J4
$\overline{T}$
$\overline{10 \div 1\,\mu s}$
$\overline{10^2 \div 10\,\mu s}$
$\overline{10^3 \div 100\,\mu s}$
$\overline{10^4 \div 1\,ms}$
$\overline{10^5 \div 10\,ms}$
$\overline{10^6 \div 100\,ms}$
$\overline{10^7 \div 1s}$
$\overline{10^8 \div 10s}$
$\overline{10^9 \div 100s}$
$\overline{GATE}$
HARMONIC COUNT
$\overline{T2}$ CLEAR
$\overline{UPDATE}$
fa/10
JUMPER USED ON 80158, 80358 W2
TI (100 ns)
TIA (10 ns)
TIA (100 ns)
DP1
DP2
DP3
DP4
DP5
DP6
DP7
DP8
MHz
KHz
SEC
NSEC
μSEC
Q1 2N3646

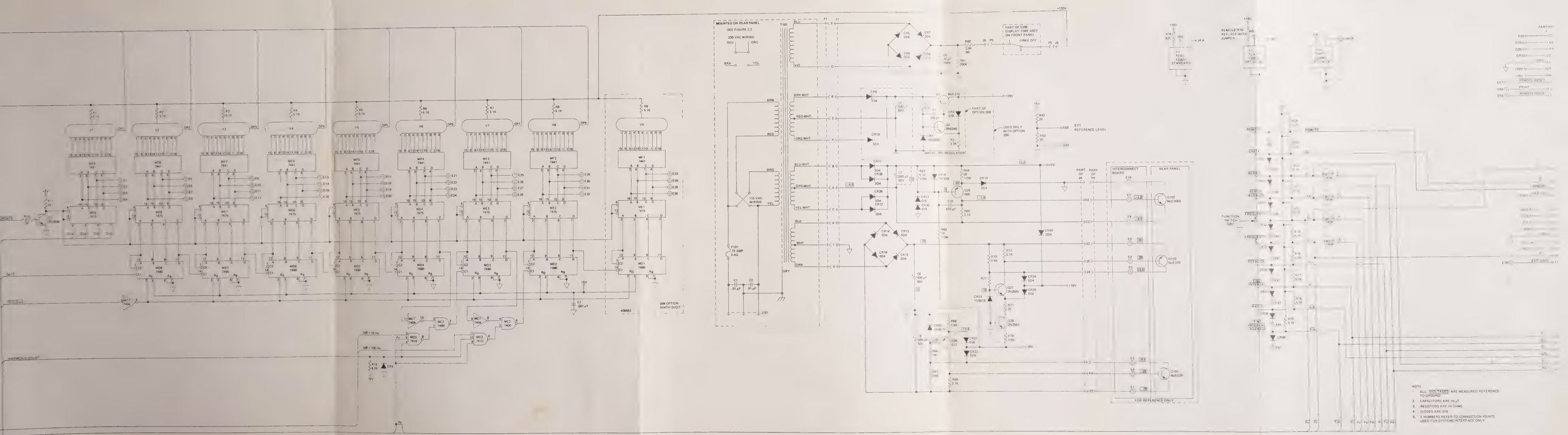


Figure 6.6 - Schematic, Readout Board 6-7

6-8 Figure 6.7 - Schematic, Interconnect Board

Field Service Bulletin No. 81-1073

2401 CAMPUS DRIVE, IRVINE, CALIFORNIA 92664 714-833-1234

11/3/70

RECEIVED
FEB 5 1971
Hytronic Measurement, Inc.
Phoenix, Arizona

SUBJECT: Model 8100 Series Counter

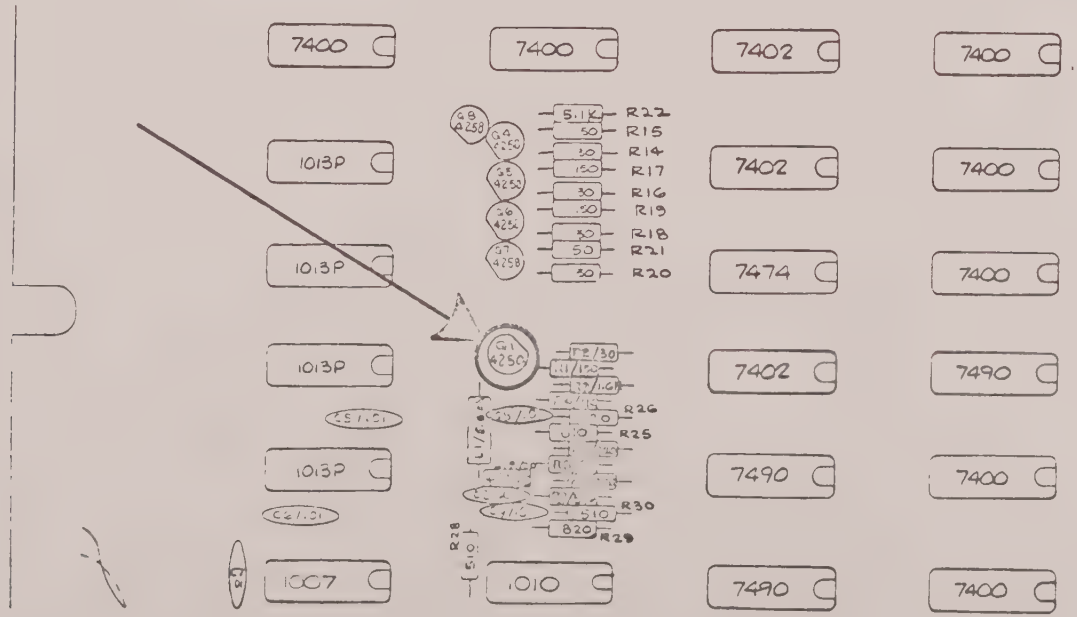
PURPOSE: Increase switching speed to allow measurement of small time intervals

ACTION: On part number 406081 High Speed Switching Assembly, replace transistor Q1 with part number 200099 Transistor, type 2N4258

EFFECTIVITY: Part number 406081 through revision K

AUTHORITY: EO 6102

PRIORITY: As required



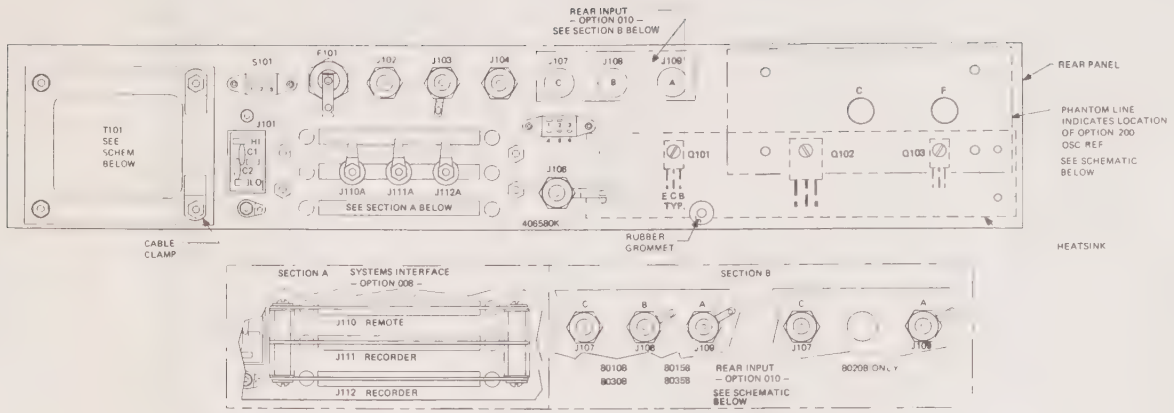


Figure 6.8 - Layout, Rear Panel

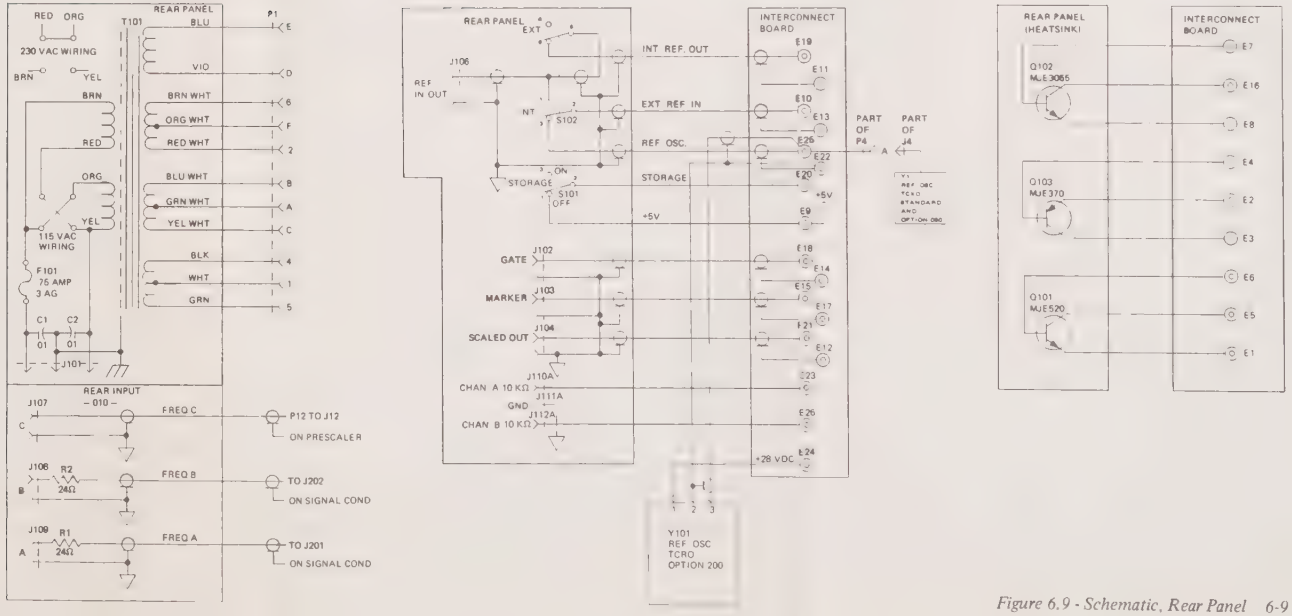


Figure 6.9 - Schematic, Rear Panel

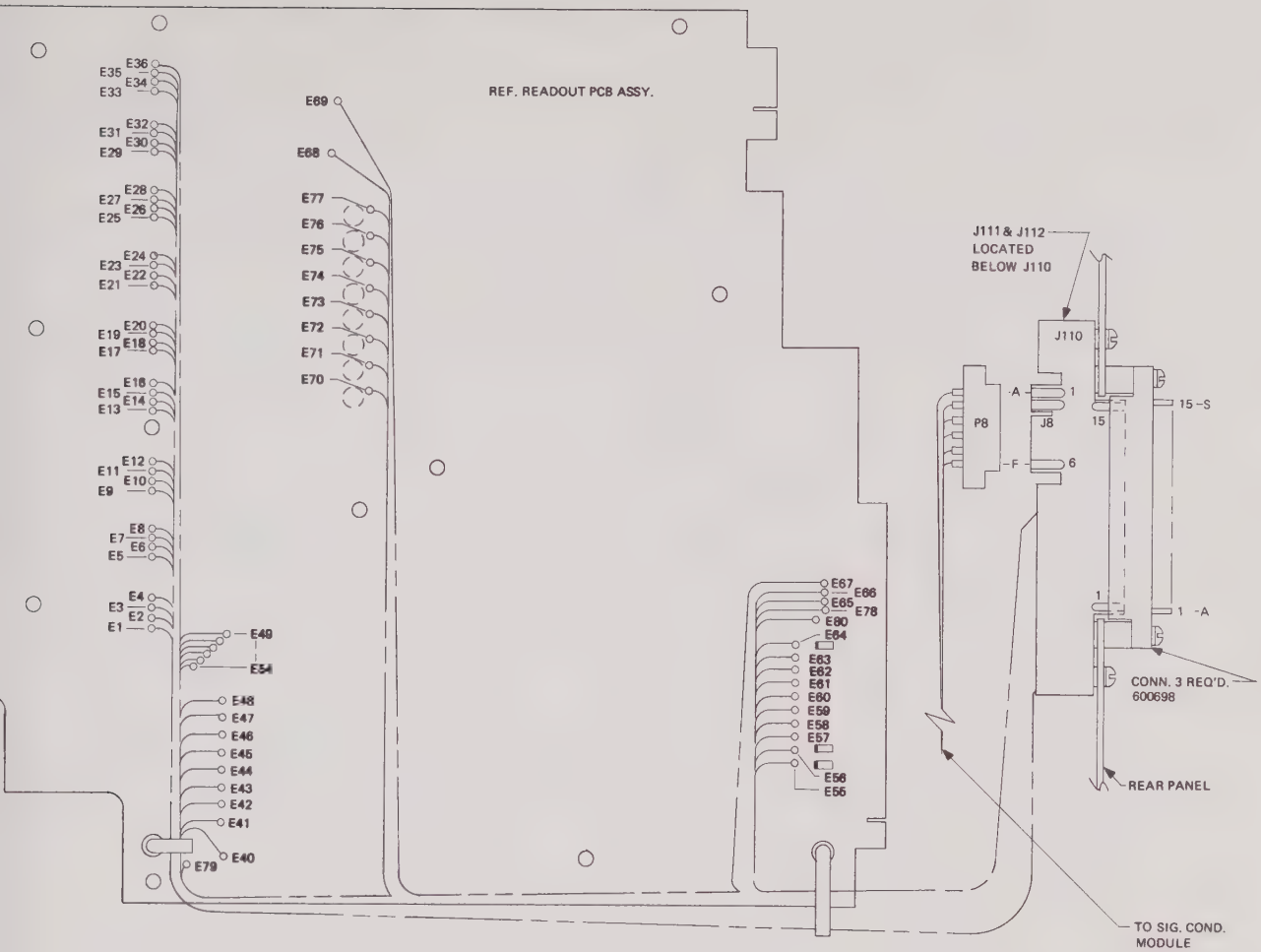


Figure 6.10 - Layout, Systems Interface

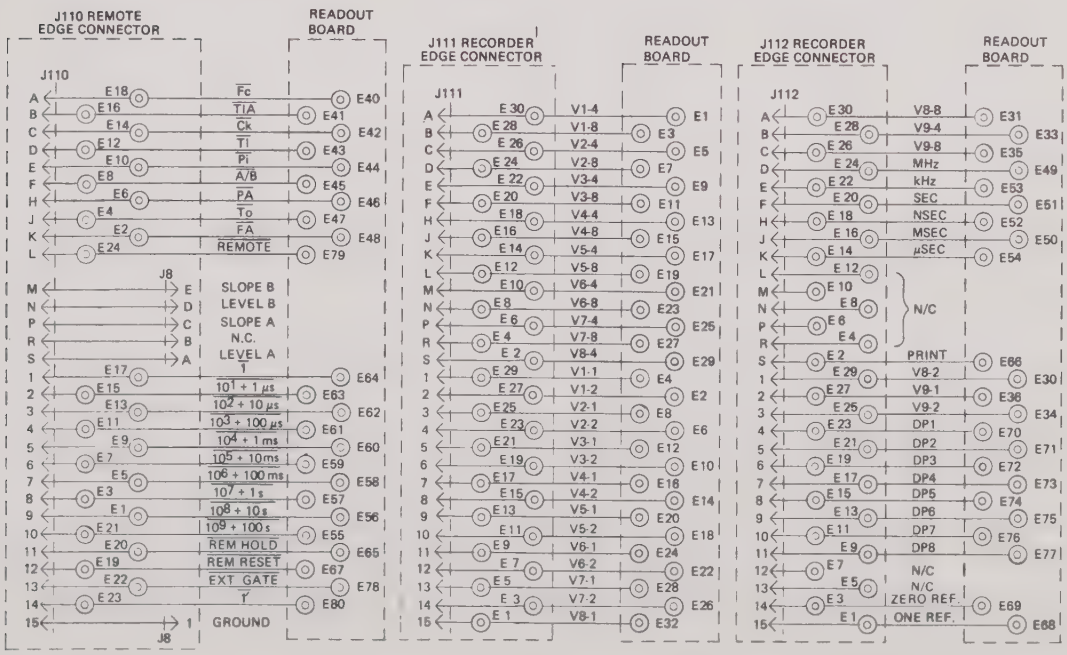


Figure 6.11 - Schematic, Systems Interface 6-11

SECTION 7 PARTS LIST

7.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

List of Suppliers 7-2
Signal Conditioning Attenuator 7-3
Signal Conditioning, PCB 7-4
Switch Board 7-8
Readout Board 7-16
Rear Panel 7-21
Display Time Control 7-22
Interconnect Board 7-23
9th Digit Readout, Option 004 7-24
Systems Interface, Option 008 7-25
Rear Input, Option 010. 7-26
TCXO Oscillator, Option 050. 7-27
TCRO Oscillator, Option 200. 7-28
28V Regulator, Option 200 7-29

7.2 Manufacturers are identified by FSC numbers listed in table 7.2, "List of Suppliers". The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks HR-1, HR-2, and their supplements.

7.3 Certain parts having 21793 (Dana) listed in the "FSC" column are specially-selected semiconductors. For some of these, standard commercial parts will serve as satisfactory replacements. These Dana parts are identified in table 7.1 along with the commercial equivalent.

Table 7.1

Semiconductor Type:		Equivalent:
007	Diode	Fairchild FD300
009	Transistor	Motorola 2N2905
014	Transistor	Motorola 2N3501
018	Diode	Texas Instruments 1N4448
021	Transistor	MPS A92

LIST OF SUPPLIERS

FSC	NAME
01295	TEXAS INSTRUMENTS, INC. DALLAS, TEXAS
02660	AMPHENOL-BORG ELECT. CORP. CHICAGO, ILLINOIS
04713	MOTOROLA, INC. (Semiconductor Products Division) PHOENIX, ARIZONA
05571	SPRAGUE ELECT. CO. (Pacific Division) LOS ANGELES, CALIFORNIA
09182	HEWLETT-PACKARD FULLERTON, CALIFORNIA
11237	CTS SOUTH PASADENA, CALIFORNIA
12060	DIODES, INC. CHATSWORTH, CALIFORNIA
21551	C-F ELECT., INC. VAN NUYS, CALIFORNIA
21793	DANA LABORATORIES, INC. IRVINE, CALIFORNIA
23095	AZTEC ELECT., INC. ANAHEIM, CALIFORNIA
27264	MOLEX PROD. CO. DOWNERS GROVE, ILLINOIS
71468	ITT SEMICONDUCTORS WAKEFIELD, MASSACHUSETTS
71471	AEROVOX CORP. (HI-Q Division) BURBANK, CALIFORNIA
71590	GLOBE UNION, INC. (Centralab Division) MILWAUKEE, WISCONSIN
71785	CINCH MFG. CO. (H. B. Jones Division) CHICAGO, ILLINOIS
72136	EL-MENCO WILLIMANTIC, CONNECTICUT
72982	ERIE TECHNOLOGICAL PROD., INC. ERIE, PENNSYLVANIA
73138	BECKMAN INSTRUMENTS FULLERTON, CALIFORNIA
73445	AMPEREX ELECT. CORP. HICKSVILLE, LONG ISLAND, NEW YORK
74276	SIGNALITE, INC. NEPTUNE, NEW JERSEY
75915	LITTLEFUSE, INC. DES PLAINES, ILLINOIS
76493	MILLER, J. W. CO. COMPTON, CALIFORNIA
79727	CONTINENTAL & WIRT ELECT. CORP. PHILADELPHIA, PENNSYLVANIA
80131	ELECTRONICS INDUSTRIES ASSOC. WASHINGTON, D. C.
81349	MILITARY SPECIFICATION
82389	SWITCHCRAFT, INC. CHICAGO, ILLINOIS
98291	SEALECTRO CORP. MAMARONECK, NEW YORK
99800	DELEVAN ELECT. CORP. AURORA, NEW YORK

406654 – Assy., ATTENUATOR, SIGNAL COND (DUAL CHANNEL)

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
B1	920563	BEADS, SHIELDING			56-59065-4B			56-59065-4B
B1A	920563	BEADS, SHIELDING			56-59065-4B			56-59065-4B
B2	920563	BEADS, SHIELDING			56-59065-4B			56-59065-4B
B2A	920563	BEADS, SHIELDING			56-59065-4B			56-59065-4B
B3	920563	BEADS, SHIELDING			56-59065-4B			56-59065-4B
B4	920563	BEADS, SHIELDING			56-59065-4B			56-59065-4B
C1	100063	CAP		.01 MFD	500 V	20%	05571	5GAS-S10
C1A	100063	CAP		.01 MFD	500 V	20%	05571	5GAS-S10
C2	101182	CAP	CERAM	47 PFD	500 V	10%	71471	TCD-N750
C2A	101182	CAP	CERAM	47 PFD	500 V	10%	71471	TCD-N750
C3	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TCD-N750
C3A	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TCD-N750
C4	100016	CAP	CERAM	27 PFD	N750		71471	N750
C4A	100016	CAP	CERAM	27 PFD	N750		71471	N750
C5	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TCD-N750
C5A	100009	CAP	CERAM	5 PFD	500 V	10%	71471	TCD-N750
C6	101182	CAP	CERAM	47 PFD	500 V	10%	71471	TCD-N750
C6A	101182	CAP	CERAM	47 PFD	500 V	10%	71471	TCD-N750
J201	600567	CONN			31-236-1050		02660	31-236-1050
J202	600567	CONN			31-236-1050		02660	31-236-1050
R1	010609	RES	METAL	909 K	T-0	1%	81349	RN60D9093F
R1A	010609	RES	METAL	909 K	T-0	1%	81349	RN60D9093F
R2	010680	RES	METAL	90.9 K		1%	81349	RN55C
R2A	010680	RES	METAL	90.9 K		1%	81349	RN55C
R3	010529	RES		10 K		1%	81349	RN55D
R3A	010529	RES		10 K		1%	81349	RN55D
R4	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R4A	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
S202A	600603	SWITCH	ATTENUATOR				11237	
S203A	600603	SWITCH	ATTENUATOR				11237	
S206	600613	SWITCH	SLIDE, SPDT		WITH .328 KNOB		79727	GF-124
S207	600613	SWITCH	SLIDE, SPDT		WITH .328 KNOB		79727	GF-124
S208	600613	SWITCH	SLIDE, SPDT		WITH .328 KNOB		79727	GF-124
S209	600613	SWITCH	SLIDE, SPDT		WITH .328 KNOB		79727	GF-124
S210	600613	SWITCH	SLIDE, SPDT		WITH .328 KNOB		79727	GF-124

406147 – Assy., PCB, SIGNAL COND (DUAL CHANNEL)

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
	715147	PC BOARD			715147	21793	715147
B1	920563	BEADS, SHIELDING			56-59065-4B		56-59065-4B
B1A	920563	BEADS, SHIELDING			56-59065-4B		56-59065-4B
B2	920563	BEADS, SHIELDING			56-59065-4B		56-59065-4B
B2A	920563	BEADS, SHIELDING			56-59065-4B		56-59065-4B
B3	920563	BEADS, SHIELDING			56-59065-4B		56-59065-4B
B3A	920563	BEADS, SHIELDING			56-59065-4B		56-59065-4B
C1	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C1A	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C2	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C2A	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C3	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C3A	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C4	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C4A	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C6	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C6A	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C7	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C7A	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C8	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C8A	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C9	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C9A	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C10	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C10A	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C11	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C11A	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C12	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
C12A	100017	CAP	CERAM	.01 MFD	100 V	05571	TH-S10
CR1	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5	04713	1/4M3.3AZ5
CR1A	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5	04713	1/4M3.3AZ5
CR2	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5	04713	1/4M3.3AZ5
CR2A	220031	DIODE	SILICO	ZENER	1/4M3.3AZ5	04713	1/4M3.3AZ5
CR3	211236	DIODE	SILICO		007	21793	211236
CR3A	211236	DIODE	SILICO		007	21793	211236
CR4	211236	DIODE	SILICO		007	21793	211236
CR4A	211236	DIODE	SILICO		007	21793	211236
CR5	220019	DIODE	SILICO	ZENER	1N752A	81349	1N752A
CR5A	220019	DIODE	SILICO	ZENER	1N752A	81349	1N752A
CR6	211083	DIODE	SILICO		018	21793	211083
CR6A	211083	DIODE	SILICO		018	21793	211083
CR7	211083	DIODE	SILICO		018	21793	211083

406147 – Assy., PCB, SIGNAL COND (DUAL CHANNEL) *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
CR7A	211083	DIODE	SILICO		018	21793	211083
CR8	220004	DIODE	SILICO	ZENER	1N961B	81349	1N961B
CR8A	220004	DIODE	SILICO	ZENER	1N961B	81349	1N961B
J6	600573	CONN			50-051-0000	98291	50-051-0000
J7	600573	CONN			50-051-0000	98291	50-051-0000
L1	310068	CHOKE		1 UH	1537-12	99800	1537-12
L1A	310068	CHOKE		1 UH	1537-12	99800	1537-12
L2	310068	CHOKE		1 UH	1537-12	99800	1537-12
L2A	310068	CHOKE		1 UH	1537-12	99800	1537-12
L3A	310101	CHOKE	RF	.27 UH	1025-06	99800	1025-06
L4A	310101	CHOKE	RF	.27 UH	1025-06	99800	1025-06
Q1	200189	TRANS	MATCHED PAIR WITH Q10			21793	200189
Q1A	200189	TRANS	MATCHED PAIR WITH Q10A			21793	200189
Q2	200186	TRANS	MATCHED PAIR WITH Q9			21793	200186
Q2A	200186	TRANS	MATCHED PAIR WITH Q9A			21793	200186
Q3	200151	TRANS			2N5179	81349	2N5179
Q3A	200151	TRANS	MATCHED PAIR WITH Q7A			81349	2N5179
Q4	200151	TRANS			2N5179	81349	2N5179
Q4A	200151	TRANS	MATCHED PAIR WITH Q8A			81349	2N5179
Q5	200151	TRANS			2N5179	81349	2N5179
Q5A	200151	TRANS			2N5179	81349	2N5179
Q6	200151	TRANS			2N5179	81349	2N5179
Q6A	200151	TRANS			2N5179	81349	2N5179
Q7	200151	TRANS			2N5179	81349	2N5179
Q7A	200151	TRANS	MATCHED PAIR WITH Q3A			81349	2N5179
Q8	200151	TRANS			2N5179	81349	2N5179
Q8A	200151	TRANS	MATCHED PAIR WITH Q4A			81349	2N5179
Q9	200186	TRANS	MATCHED PAIR WITH Q2			21793	200186
Q9A	200186	TRANS	MATCHED PAIR WITH Q2A			21793	200186
Q10	200189	TRANS	MATCHED PAIR WITH Q1			21793	200189
Q10A	200189	TRANS	MATCHED PAIR WITH Q1A			21793	200189
Q11	200043	TRANS	SILICO	NPN	2N3565	80131	2N3565
Q11A	200043	TRANS	SILICO	NPN	2N3565	80131	2N3565
Q12	200043	TRANS	SILICO	NPN	2N3565	80131	2N3565
Q12A	200043	TRANS	SILICO	NPN	2N3565	80131	2N3565
Q13	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q13A	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q14	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q14A	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
P9	600593	CONN	6 PIN		250-06-30-170	71785	250-06-30-170

406147 – Assy., PCB, SIGNAL COND (DUAL CHANNEL) *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R1	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R1A	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R2	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R2A	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R3	010720	RES	METAL	9.09 K		.25%	81349	RN55C
R3A	010720	RES	METAL	9.09 K		.25%	81349	RN55C
R4	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R4A	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R5	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R5A	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R6	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R6A	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R7	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R7A	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R8	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R8A	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R9A	000152	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R10	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R10A	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R11	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R11A	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R12	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R12A	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R13	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R13A	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R14	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R14A	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R15A	000152	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R16	001758	RES	CARBON	330 OHM		5% 1W	81349	RC32GF331J
R16A	001758	RES	CARBON	330 OHM		5% 1W	81349	RC32GF331J
R17	040114	RES	VARI	50 K		10%	73138	62PR50
R17A	040114	RES	VARI	50 K		10%	73138	62PR50
R18	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R18A	000910	RES	CARBON	91 OHM		5% 1/4W	81349	RC07GF910J
R19	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R19A	000470	RES	CARBON	47 OHM		5% 1/4W	81349	RC07GF470J
R20	040123	RES	VARI	1 K	62PR1K		73138	62PR1K
R20A	040123	RES	VARI	1 K	62PR1K		73138	62PR1K
R21	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R21A	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R22	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R22A	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R23	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R23A	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R24	010720	RES	METAL	9.09 K		.25%	81349	RN55C

406147 – Assy., PCB, SIGNAL COND (DUAL CHANNEL) *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R24A	010720	RES	METAL	9.09 K		.25%	81349	RN55C
R25	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R25A	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R26	010704	RES	METAL	1 K	T-0	1%	81349	RN55D1001F
R26A	010704	RES	METAL	1 K	T-0	1%	81349	RN55D1001F
R27	010630	RES	METAL	9.09 K		1%	81349	RN55D9091F
R27A	010630	RES	METAL	9.09 K		1%	81349	RN55D9091F
R28	000682	RES	CARBON	9.8 M		1%		DCS1/2
R28A	000682	RES	CARBON	9.8 M		1%		DCS1/2
R29	000682	RES	CARBON	9.8 M		1%		DCS1/2
R29A	000682	RES	CARBON	9.8 M		1%		DCS1/2
R30	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R30A	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R31	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R31A	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R32	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R32A	000203	RES	CARBON	20 K		5% 1/4W	81349	RC07GF203J
R33	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R33A	010705	RES	METAL	4.53 K	T-0	1%	81349	RN55D4531F
R34	040212	POT		25 K	UPE200-25K		11237	UPE200-25K
R34A	040212	POT		25 K	UPE200-25K		11237	UPE200-25K
R35	000391	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J
R35A	000391	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J
R36	000241	RES	CARBON	240 OHM		5% 1/4W	81349	RC07GF241J
R36A	000241	RES	CARBON	240 OHM		5% 1/4W	81349	RC07GF241J
R37	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R37A	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R38	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R38A	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
S202B		SWITCH	(PART OF R34 & R34A)					
S203B		SWITCH	(PART OF R34 & R34A)					
W1	600245	JUMPER			L-2007-1			L-2007-1
W2	600245	JUMPER			L-2007-1			L-2007-1

406151 – Assy., PCB, SWITCH BOARD

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
	715151	PC BOARD			715151		21793	715151
C1	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C2	100069	CAP	CERAM	20 PFD	1000 V	20%	05571	C023B102E220M
C3	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C4	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C5	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C6	100003	CAP	CERAM	3.3 PFD	DD3R3		71590	DD3R3
C7	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C8	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C9	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C10	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C11	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C12	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C13	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C14	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C15	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C20	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C21	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C22	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C23	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C25	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C26	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C27	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C28	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C29	110104	CAP	TANT	4.7 MFD	10 V	10%		K4R7C10K
C30	100012	CAP	CERAM	33 PFD	500 V	10%	71471	TCD-N750
C31	100068	CAP	CERAM	.02 MFD	100 V	20%	05571	TG-S20
C32	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C35	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C36	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C37	130082	CAP	MICA	110 PFD	DM5-F111G		72136	DM5-F111G
C38	130111	CAP	MICA	91 PFD	500 V	5%	72136	DM10-910J
C39	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C40	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C41	100050	CAP			10TCC-V22		05571	10TCC-V22
C42	100051	CAP		25 PFD	500 V		71471	TCD-D1-0
C43	100060	CAP			10TCC-Q15		05571	10TCC-Q15
C44	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C45	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C46	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C47	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C48	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C49	100006	CAP	CERAM	10 PFD	500 V	10%	71471	TCD-N750
C50	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10

406151 – Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C51	100061	CAP	DISC	39 PFD	1000 V	5%	05571	10TCC-Q39
C52	100061	CAP	DISC	39 PFD	1000 V	5%	05571	10TCC-Q39
C53	100040	CAP		200 PFD	5GA-T20		05571	5GA-T20
C54	130101	CAP			538-011D9-35		72982	538-011D9-35
C55	100068	CAP	CERAM	.02 MFD	100 V	20%	05571	TG-S20
C56	130101	CAP			538-011D9-35		72982	538-011D9-35
C57	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C58	100040	CAP		200 PFD	5GA-T20		05571	5GA-T20
C59	100017	CAP	CERAM	.01 MFD	100 V		05571	TH-S10
C60	100040	CAP		200 PFD	5GA-T20		05571	5GA-T20
C61	110144	CAP	TANT	10 MFD	10 V		71468	
CR1	211083	DIODE	SILICO		018		21793	211083
CR2	211083	DIODE	SILICO		018		21793	211083
CR5	211083	DIODE	SILICO		018		21793	211083
CR6	211083	DIODE	SILICO		018		21793	211083
CR7	211083	DIODE	SILICO		018		21793	211083
CR8	211083	DIODE	SILICO		018		21793	211083
CR9	211083	DIODE	SILICO		018		21793	211083
CR10	211083	DIODE	SILICO		018		21793	211083
CR11	211083	DIODE	SILICO		018		21793	211083
CR12	211083	DIODE	SILICO		018		21793	211083
CR13	211083	DIODE	SILICO		018		21793	211083
CR14	211083	DIODE	SILICO		018		21793	211083
CR15	211083	DIODE	SILICO		018		21793	211083
CR16	211083	DIODE	SILICO		018		21793	211083
CR17	211083	DIODE	SILICO		018		21793	211083
CR18	211083	DIODE	SILICO		018		21793	211083
CR19	211083	DIODE	SILICO		018		21793	211083
CR20	211083	DIODE	SILICO		018		21793	211083
CR21	211083	DIODE	SILICO		018		21793	211083
CR22	211083	DIODE	SILICO		018		21793	211083
CR23	211083	DIODE	SILICO		018		21793	211083
CR25	211083	DIODE	SILICO		018		21793	211083
CR26	211083	DIODE	SILICO		018		21793	211083
CR27	211083	DIODE	SILICO		018		21793	211083
CR28	211083	DIODE	SILICO		018		21793	211083
CR29	211083	DIODE	SILICO		018		21793	211083
CR30	211083	DIODE	SILICO		018		21793	211083
CR35	211083	DIODE	SILICO		018		21793	211083
CR36	211083	DIODE	SILICO		018		21793	211083
CR37	211083	DIODE	SILICO		018		21793	211083
CR38	211083	DIODE	SILICO		018		21793	211083
CR40	211083	DIODE	SILICO		018		21793	211083
CR41	211083	DIODE	SILICO		018		21793	211083

406151 – Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
CR42	210015	DIODE			HP5082-2800	09182	HP5082-2800
CR43	210015	DIODE			HP5082-2800	09182	HP5082-2800
CR45	211083	DIODE	SILICO		018	21793	211083
CR46	211083	DIODE	SILICO		018	21793	211083
CR47	211083	DIODE	SILICO		018	21793	211083
CR48	211083	DIODE	SILICO		018	21793	211083
CR49	211083	DIODE	SILICO		018	21793	211083
CR50	211083	DIODE	SILICO		018	21793	211083
CR51	211083	DIODE	SILICO		018	21793	211083
CR52	211083	DIODE	SILICO		018	21793	211083
CR53	211083	DIODE	SILICO		018	21793	211083
CR54	211083	DIODE	SILICO		018	21793	211083
L1	310091	CHOKE		68 UH	1537-68	99800	1537-68
L2	310062	CHOKE	RF	22 UH	1537-44	99800	1537-44
L4	310090	CHOKE		.56 UH	1537-07	99800	1537-07
L5	310062	CHOKE	RF	22 UH	1537-44	99800	1537-44
L6	310090	CHOKE		.56 UH	1537-07	99800	1537-07
L7	310062	CHOKE	RF	22 UH	1537-44	99800	1537-44
L8	310092	CHOKE	RF	.10 UH	9230-94	76493	9230-94
L9	310088	CHOKE	RF	.15 UH	1537-00	99800	1537-00
L10	920563	BEADS, SHIELDING			56-59065-4B		56-59065-4B
MA1	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MA7	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MA8	230099	INTEGRATED CIRCUIT			SN7454N	01295	SN7454N
MA9	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
MA10	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
MB6	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MB7	230072	INTEGRATED CIRCUIT			SN7474N	01295	SN7474N
MB8	230064	INTEGRATED CIRCUIT			SN7404N	01295	SN7404N
MB9	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
MB10	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
MC1	230039	INTEGRATED CIRCUIT			MC1023P	04713	MC1023P
MC2	230043	INTEGRATED CIRCUIT			MC1010P	04713	MC1010P
MC5	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MC6	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MC8	230099	INTEGRATED CIRCUIT			SN7454N	01295	SN7454N
MC9	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
MC10	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
MD1	230039	INTEGRATED CIRCUIT			MC1023P	04713	MC1023P
MD2	230097	INTEGRATED CIRCUIT			MC1034P	04713	MC1034P
MD3	230096	INTEGRATED CIRCUIT			MC1032P	04713	MC1032P
MD4	230048	INTEGRATED CIRCUIT			MC1027P	04713	MC1027P
MD5	230030	INTEGRATED CIRCUIT			SN7402N	01295	SN7402N

406151 – Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
MD6	230064	INTEGRATED CIRCUIT			SN7404N	01295	SN7404N
MD7	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MD8	230064	INTEGRATED CIRCUIT			SN7404N	01295	SN7404N
MD9	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
MD10	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
ME1	230039	INTEGRATED CIRCUIT			MC1023P	04713	MC1023P
ME2	230113	INTEGRATED CIRCUIT			MC1034P	04713	MC1034P
ME3	230113	INTEGRATED CIRCUIT			MC1034P	04713	MC1034P
ME4	230040	INTEGRATED CIRCUIT			MC1013P	04713	MC1013P
ME5	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
ME6	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
ME7	230030	INTEGRATED CIRCUIT			SN7402N	01295	SN7402N
ME8	230032	INTEGRATED CIRCUIT			SN7420N	01295	SN7420N
ME9	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
ME10	230037	INTEGRATED CIRCUIT			SN7490N	01295	SN7490N
MF3	230040	INTEGRATED CIRCUIT			MC1013P	04713	MC1013P
MF4	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MF5	230031	INTEGRATED CIRCUIT			SN7410N	01295	SN7410N
MF6	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MF7	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
MF8	230099	INTEGRATED CIRCUIT			SN7454N	01295	SN7454N
MF9	230072	INTEGRATED CIRCUIT			SN7474N	01295	SN7474N
MF10	230028	INTEGRATED CIRCUIT			SN7400N	01295	SN7400N
P6	600483	CONN	COAX		27-7	02660	27-7
P7	600483	CONN	COAX		27-7	02660	27-7
P13	600483	CONN	COAX		27-7	02660	27-7
Q1	200099	TRANS			2N4258	81349	2N4258
Q2	200099	TRANS			2N4258	81349	2N4258
Q3	200099	TRANS			2N4258	81349	2N4258
Q4	200099	TRANS			2N4258	81349	2N4258
Q5	200099	TRANS			2N4258	81349	2N4258
Q6	200099	TRANS			2N4258	81349	2N4258
Q7	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q8	200099	TRANS			2N4258	81349	2N4258
Q9	200088	TRANS	SILICO	PNP	2N4248	80131	2N4248
Q10	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q11	200099	TRANS			2N4258	81349	2N4258
Q12	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q13	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q14	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q15	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q16	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646
Q17	200037	TRANS	SILICO	NPN	2N3646	80131	2N3646

406151 – Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
Q18	200071	TRANS	SILICO		2N3563		81349	2N3563
Q19	200071	TRANS	SILICO		2N3563		81349	2N3563
Q20	200088	TRANS	SILICO	PNP	2N4248		80131	2N4248
Q21	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
Q22	200068	TRANS			2N4250		80131	2N4250
R1	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R2	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R3	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R4	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R5	000200	RES	CARBON	20 OHM		5% 1/4W	81349	RC07GF200J
R6	000750	RES	CARBON	75 OHM		5% 1/4W	81349	RC07GF750J
R7	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R8	000471	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
R9	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R10	000621	RES	CARBON	620 OHM		5% 1/4W	81349	RC07GF621J
R11	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R12	000240	RES	CARBON	24 OHM		5% 1/4W	81349	RC07GF240J
R13	000750	RES	CARBON	75 OHM		5% 1/4W	81349	RC07GF750J
R14	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R15	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R16	000152	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R17	000821	RES	CARBON	820 OHM		5% 1/4W	81349	RC07GF821J
R18	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R19	000112	RES	CARBON	1.1 K		5% 1/4W	81349	RC07GF112J
R20	000621	RES	CARBON	620 OHM		5% 1/4W	81349	RC07GF621J
R21	000621	RES	CARBON	620 OHM		5% 1/4W	81349	RC07GF621J
R22	000301	RES	CARBON	300 OHM		5% 1/4W	81349	RC07GF301J
R23	000391	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J
R24	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R25	000301	RES	CARBON	300 OHM		5% 1/4W	81349	RC07GF301J
R26	000242	RES	CARBON	2.4 K		5% 1/4W	81349	RC07GF242J
R27	000182	RES	CARBON	1.8 K		5% 1/4W	81349	RC07GF182J
R28	000391	RES	CARBON	390 OHM		5% 1/4W	81349	RC07GF391J
R29	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R30	000750	RES	CARBON	75 OHM		5% 1/4W	81349	RC07GF750J
R31	000240	RES	CARBON	24 OHM		5% 1/4W	81349	RC07GF240J
R32	000750	RES	CARBON	75 OHM		5% 1/4W	81349	RC07GF750J
R33	000240	RES	CARBON	24 OHM		5% 1/4W	81349	RC07GF240J
R34	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R35	000472	RES	CARBON	4.7 K		5% 1/4W	81349	RC07GF472J
R36	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R37	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R40	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J
R41	000222	RES	CARBON	2.2 K		5% 1/4W	81349	RC07GF222J

406151 – Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R42	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R43	000471	RES	CARBON	470 OHM	5% 1/4W	81349	RC07GF471J
R44	000471	RES	CARBON	470 OHM	5% 1/4W	81349	RC07GF471J
R45	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R46	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R47	000471	RES	CARBON	470 OHM	5% 1/4W	81349	RC07GF471J
R48	000222	RES	CARBON	2.2 K	5% 1/4W	81349	RC07GF222J
R49	000222	RES	CARBON	2.2 K	5% 1/4W	81349	RC07GF222J
R50	000222	RES	CARBON	2.2 K	5% 1/4W	81349	RC07GF222J
R51	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R52	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R53	000112	RES	CARBON	1.1 K	5% 1/4W	81349	RC07GF112J
R54	000112	RES	CARBON	1.1 K	5% 1/4W	81349	RC07GF112J
R55	000112	RES	CARBON	1.1 K	5% 1/4W	81349	RC07GF112J
R56	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R57	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R58	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R59	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R60	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R61	000242	RES	CARBON	2.4 K	5% 1/4W	81349	RC07GF242J
R62	000242	RES	CARBON	2.4 K	5% 1/4W	81349	RC07GF242J
R63	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R64	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R65	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R66	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R67	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R68	000123	RES	CARBON	12 K	5% 1/4W	81349	RC07GF123J
R69	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R70	000200	RES	CARBON	20 OHM	5% 1/4W	81349	RC07GF200J
R71	000750	RES	CARBON	75 OHM	5% 1/4W	81349	RC07GF750J
R72	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R73	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R74	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R75	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R76	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R77	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R78	000471	RES	CARBON	470 OHM	5% 1/4W	81349	RC07GF471J
R79	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R80	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R81	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R82	000472	RES	CARBON	4.7 K	5% 1/4W	81349	RC07GF472J
R83	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R84	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R85	000510	RES	CARBON	51 OHM	5% 1/4W	81349	RC07GF510J
R86	000200	RES	CARBON	20 OHM	5% 1/4W	81349	RC07GF200J

406151 – Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R87	000750	RES	CARBON	75 OHM	5% 1/4W	81349	RC07GF750J
R88	000270	RES	CARBON	27 OHM	5% 1/4W	81349	RC07GF270J
R89	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R90	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R91	000122	RES	CARBON	1.2 K	5% 1/4W	81349	RC07GF122J
R92	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R93	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R94	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R95	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R96	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R97	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R98	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R99	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R100	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R101	000162	RES	CARBON	1.6 K	5% 1/4W	81349	RC07GF162J
R102	000122	RES	CARBON	1.2 K	5% 1/4W	81349	RC07GF122J
R105	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R106	000510	RES	CARBON	51 OHM	5% 1/4W	81349	RC07GF510J
R107	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R108	000100	RES	CARBON	10 OHM	5% 1/4W	81349	RC07GF100J
R109	000332	RES	CARBON	3.3 K	5% 1/4W	81349	RC07GF332J
R110	000151	RES	CARBON	150 OHM	5% 1/4W	81349	RC07GF151J
R111	000300	RES	CARBON	30 OHM	5% 1/4W	81349	RC07GF300J
R112	000681	RES	CARBON	680 OHM	5% 1/4W	81349	RC07GF681J
R113	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R117	000200	RES	CARBON	20 OHM	5% 1/4W	81349	RC07GF200J
R118	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R119	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R120	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R121	000390	RES	CARBON	39 OHM	5% 1/4W	81349	RC07GF390J
R122	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R123	000301	RES	CARBON	300 OHM	5% 1/4W	81349	RC07GF301J
R124	000472	RES	CARBON	4.7 K	5% 1/4W	81349	RC07GF472J
R125	000821	RES	CARBON	820 OHM	5% 1/4W	81349	RC07GF821J
R126	000511	RES	CARBON	510 OHM	5% 1/4W	81349	RC07GF511J
R127	000302	RES	CARBON	3 K	5% 1/4W	81349	RC07GF302J
R128	000222	RES	CARBON	2.2 K	5% 1/4W	81349	RC07GF222J
R129	000472	RES	CARBON	4.7 K	5% 1/4W	81349	RC07GF472J
R130	000750	RES	CARBON	75 OHM	5% 1/4W	81349	RC07GF750J
R131	000510	RES	CARBON	51 OHM	5% 1/4W	81349	RC07GF510J
R132	000200	RES	CARBON	20 OHM	5% 1/4W	81349	RC07GF200J
R133	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R134	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R135	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R136	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J

406151 – Assy., PCB, SWITCH BOARD *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R137	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R138	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R139	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R140	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R141	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R142	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
S1	600605	SWITCH 10 SEGMENT INTERLOCKED (A - L)	71590	C18-PB101L
S2	600604	SWITCH (A & B)	71590	C18-PB2M
W2	600245	JUMPER L-2007-1		L-2007-1
Y1	920583	CRYSTAL 9998.800 KHz 920583	21793	920583

406146 – Assy., PCB, READOUT BOARD

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
	715145	PC BOARD			715145		21793	715145
C1	101174	CAP	CERAM	.001 MFD	500 V	10%	71471	SCD3X5F
C5	110131	CAP		20 MFD	450 V		05571	39D206F450GL4
C7	110146	CAP		5000 MFD	10 V	20%	05571	39D508G010HP4
C8	110062	CAP	ELECT	500 MFD	50 V		05571	39D507G050L4
C9	110062	CAP	ELECT	500 MFD	50 V		05571	39D507G050L4
C10	101641	CAP	CERAM	470 PFD	500 V	10%	71471	SCD1X5F
CR1	211083	DIODE	SILICO		018		21793	211083
CR2	211083	DIODE	SILICO		018		21793	211083
CR3	211083	DIODE	SILICO		018		21793	211083
CR4	211083	DIODE	SILICO		018		21793	211083
CR5	210004	DIODE	SILICO		SD4		12060	SD4
CR6	210004	DIODE	SILICO		SD4		12060	SD4
CR7	210004	DIODE	SILICO		SD4		12060	SD4
CR8	210004	DIODE	SILICO		SD4		12060	SD4
CR11	210004	DIODE	SILICO		SD4		12060	SD4
CR12	210004	DIODE	SILICO		SD4		12060	SD4
CR13	210004	DIODE	SILICO		SD4		12060	SD4
CR14	210004	DIODE	SILICO		SD4		12060	SD4
CR15	210004	DIODE	SILICO		SD4		12060	SD4
CR16	210004	DIODE	SILICO		SD4		12060	SD4
CR17	211083	DIODE	SILICO		018		21793	211083
CR18	220007	DIODE	SILICO	ZENER	1N751		81349	1N751
CR19	210004	DIODE	SILICO		SD4		12060	SD4
CR20	220015	DIODE	SILICO	ZENER	1N967B		81349	1N967B
CR21	211083	DIODE	SILICO		018		21793	211083
CR22	210004	DIODE	SILICO		SD4		12060	SD4
CR23	220015	DIODE	SILICO	ZENER	1N967B		81349	1N967B
CR24	210004	DIODE	SILICO		SD4		12060	SD4
CR25	211083	DIODE	SILICO		018		21793	211083
CR26	211083	DIODE	SILICO		018		21793	211083
CR27	211083	DIODE	SILICO		018		21793	211083
CR28	210004	DIODE	SILICO		SD4		12060	SD4
CR29	210004	DIODE	SILICO		SD4		12060	SD4
CR30	211083	DIODE	SILICO		018		21793	211083
CR40	210004	DIODE	SILICO		SD4		12060	SD4
D1	920602	NEON	BULB		A1C-A		74276	A1C-A
D2	920602	NEON	BULB		A1C-A		74276	A1C-A
D3	920602	NEON	BULB		A1C-A		74276	A1C-A
D4	920602	NEON	BULB		A1C-A		74276	A1C-A
D5	920602	NEON	BULB		A1C-A		74276	A1C-A
D6	920602	NEON	BULB		A1C-A		74276	A1C-A

406146 – Assy., PCB, READOUT BOARD *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
D7	920602	NEON BULB A1C-A	74276	A1C-A
J5	600665	TERM BOARD PIN .062 DIA R62-3		R62-3
MA7	230064	INTEGRATED CIRCUIT SN7404N	01295	SN7404N
MA8	230031	INTEGRATED CIRCUIT SN7410N	01295	SN7410N
MA9	230099	INTEGRATED CIRCUIT SN7454N	01295	SN7454N
MA10	230099	INTEGRATED CIRCUIT SN7454N	01295	SN7454N
MA11	230031	INTEGRATED CIRCUIT SN7410N	01295	SN7410N
MA12	230064	INTEGRATED CIRCUIT SN7404N	01295	SN7404N
MB7	230064	INTEGRATED CIRCUIT SN7404N	01295	SN7404N
MB8	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
MB9	230099	INTEGRATED CIRCUIT SN7454N	01295	SN7454N
MB10	230099	INTEGRATED CIRCUIT SN7454N	01295	SN7454N
MB11	230031	INTEGRATED CIRCUIT SN7410N	01295	SN7410N
MB12	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
MC1	230064	INTEGRATED CIRCUIT SN7404N	01295	SN7404N
MC2	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
MC3	230031	INTEGRATED CIRCUIT SN7410N	01295	SN7410N
MC7	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
MC8	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
MC9	230098	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MC10	230098	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MC11	230098	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MC12	230099	INTEGRATED CIRCUIT SN7454N	01295	SN7454N
MD2	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MD3	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MD4	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MD5	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MD6	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MD7	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MD8	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
MD10	230064	INTEGRATED CIRCUIT SN7404N	01295	SN7404N
MD11	230028	INTEGRATED CIRCUIT SN7400N	01295	SN7400N
MD12	230099	INTEGRATED CIRCUIT SN7454N	01295	SN7454N
ME2	230065	INTEGRATED CIRCUIT SN7475N	01295	SN7475N
ME3	230065	INTEGRATED CIRCUIT SN7475N	01295	SN7475N
ME4	230065	INTEGRATED CIRCUIT SN7475N	01295	SN7475N
ME5	230065	INTEGRATED CIRCUIT SN7475N	01295	SN7475N
ME6	230065	INTEGRATED CIRCUIT SN7475N	01295	SN7475N
ME7	230065	INTEGRATED CIRCUIT SN7475N	01295	SN7475N
ME8	230065	INTEGRATED CIRCUIT SN7475N	01295	SN7475N
ME9	230065	INTEGRATED CIRCUIT SN7475N	01295	SN7475N
MF2	230034	INTEGRATED CIRCUIT SN7441N	01295	SN7441N
MF3	230034	INTEGRATED CIRCUIT SN7441N	01295	SN7441N

406146 – Assy., PCB, READOUT BOARD *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
MF4	230034	INTEGRATED CIRCUIT SN7441N	01295	SN7441N
MF5	230034	INTEGRATED CIRCUIT SN7441N	01295	SN7441N
MF6	230034	INTEGRATED CIRCUIT SN7441N	01295	SN7441N
MF7	230034	INTEGRATED CIRCUIT SN7441N	01295	SN7441N
MF8	230034	INTEGRATED CIRCUIT SN7441N	01295	SN7441N
MF9	230034	INTEGRATED CIRCUIT SN7441N	01295	SN7441N
Q1	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q5	200087	TRANS SILICO 021	04713	SPS1226
Q6	200087	TRANS SILICO 021	04713	SPS1226
Q7	200087	TRANS SILICO 021	04713	SPS1226
Q8	200087	TRANS SILICO 021	04713	SPS1226
Q9	200087	TRANS SILICO 021	04713	SPS1226
Q10	200087	TRANS SILICO 021	04713	SPS1226
Q11	200087	TRANS SILICO 021	04713	SPS1226
Q12	200037	TRANS SILICO NPN 2N3646	80131	2N3646
Q15	200087	TRANS SILICO 021	04713	SPS1226
Q17	200087	TRANS SILICO 021	04713	SPS1226
Q18	200087	TRANS SILICO 021	04713	SPS1226
Q19	200087	TRANS SILICO 021	04713	SPS1226
Q20	200087	TRANS SILICO 021	04713	SPS1226
Q21	200087	TRANS SILICO 021	04713	SPS1226
Q22	200087	TRANS SILICO 021	04713	SPS1226
Q23	200087	TRANS SILICO 021	04713	SPS1226
Q25	200052	TRANS SILICO PNP 009	21793	200052
Q26	200022	TRANS SILICO PNP 012	21793	200022
Q27	200043	TRANS SILICO NPN 2N3565	80131	2N3565
Q28	200043	TRANS SILICO NPN 2N3565	80131	2N3565
R1	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R2	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R3	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R4	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R5	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R6	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R7	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R8	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R10	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R11	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R12	000622	RES CARBON 6.2 K 5% 1/4W	81349	RC07GF622J
R15	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R16	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R17	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R18	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R19	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J

406146 – Assy., PCB, READOUT BOARD *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R20	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R21	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R22	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R23	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R24	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R26	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R28	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R30	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R32	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R34	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R36	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R39	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R40	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R41	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R42	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R43	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R45	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R46	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R47	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R48	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R49	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R50	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R51	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R52	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R53	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R54	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R55	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R56	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R57	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R60	020620	RES	WW	3.9 K	5%	21551	M20
R61	000204	RES	CARBON	200 K	5% 1/4W	81349	RC07GF204J
R62	000512	RES	CARBON	5.1 K	5% 1/4W	81349	RC07GF512J
R63	001793	RES	CARBON	1 K	5% 1/2W		
R64	001765	RES		68 OHM	5% 1/2W	81349	RC07GF680J
R65	000272	RES	CARBON	2.7 K	5% 1/4W	81349	RC07GF272J
R66	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R67	000362	RES	CARBON	3.6 K	5% 1/4W	81349	RC07GF362J
R68	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R69	000272	RES	CARBON	2.7 K	5% 1/4W	81349	RC07GF272J
R70	000242	RES	CARBON	2.4 K	5% 1/4W	81349	RC07GF242J
R71	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R72	000272	RES	CARBON	2.7 K	5% 1/4W	81349	RC07GF272J
R73	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R74	000152	RES	CARBON	1.5 K	5% 1/4W	81349	RC07GF152J
R75	000123	RES	CARBON	12 K	5% 1/4W	81349	RC07GF123J

406146 – Assy., PCB, READOUT *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R76	000821	RES	CARBON	820 OHM		5% 1/4W	81349	RC07GF821J
R77	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
V1	920506	TUBE	DISPLAY		ZM1000		73445	ZM1000
V2	920506	TUBE	DISPLAY		ZM1000		73445	ZM1000
V3	920506	TUBE	DISPLAY		ZM1000		73445	ZM1000
V4	920506	TUBE	DISPLAY		ZM1000		73445	ZM1000
V5	920506	TUBE	DISPLAY		ZM1000		73445	ZM1000
V6	920506	TUBE	DISPLAY		ZM1000		73445	ZM1000
V7	920506	TUBE	DISPLAY		ZM1000		73445	ZM1000
V8	920506	TUBE	DISPLAY		ZM1000		73445	ZM1000
W2	600245	JUMPER			L-2007-1			L-2007-1
W3	600245	JUMPER			L-2007-1			L-2007-1

406580 – Assy., PCB, REAR PANEL

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
	730377	REAR PANEL 730377	21793	730377
	730423	HEATSINK 730423	21793	730423
C1	100063	CAP .01 MFD 500 V 20%	05571	5GAS-S10
C2	100063	CAP .01 MFD 500 V 20%	05571	5GAS-S10
F101	920364	FUSE 1 AMP 313001	75915	313001
J101	600619	CONN RECPTLE AC POWER	82389	EAC-301
J102	600567	CONN 31-236-1050	02660	31-236-1050
J103	600567	CONN 31-236-1050	02660	31-236-1050
J104	600567	CONN 31-236-1050	02660	31-236-1050
J106	600567	CONN 31-236-1050	02660	31-236-1050
J110	600589	POST BINDING RED 820-65		820-65
J111	600586	POST BINDING WHITE 820-25		820-25
J112	600587	POST BINDING BLK 820-45		820-45
P1	600566	CONN 6 PIN 251-06-30-160	71785	251-06-30-160
Q101	200155	TRANS MJE520	04713	MJE520
Q102	200130	TRANS MJE3055	04713	MJE3055
Q103	200154	TRANS MJE370	04713	MJE370
S101	600680	SWITCH SLIDE GF-124	79727	GF-124
S102	600617	SWITCH SLIDE, DPDT G126	79727	G126
T101	300065	TRANSFORMER 11824	23095	11824

406561 – Assy., PCB, DISPLAY TIME CONTROL

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
P3	600593	CONN	6 PIN		250-06-30-170	71785	250-06-30-170
	600250	KEY					
P5	600545	PLUG	3 PIN		1625-3P-1	27264	1625-3P-1
	600381	PIN	FEMALE	2 REQ'D.			
R1		POT		1 MEG	(PART OF 600600)		
S205	600600	SWITCH	ROTARY			11237	

406128 – Assy., PCB, INTERCONNECT BOARD

REF DES	DANA P/N	DESCRIPTION			FSC	MANU P/N
	715128	PC BOARD		715128	21793	715128
P2	600575	CONN	25 PIN	252-25-30-160	71785	252-25-30-160
P4	600575	CONN	25 PIN	252-25-30-160	71785	252-25-30-160

406663 – Assy., PCB, 9 DIGIT READOUT, OPTION 004

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
MD1	230037	INTEGRATED CIRCUIT SN7490N	01295	SN7490N
ME1	230065	INTEGRATED CIRCUIT SN7475N	01295	SN7475N
MF1	230034	INTEGRATED CIRCUIT SN7441N	01295	SN7441N
R9	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
V9	920506	TUBE DISPLAY ZM1000	73445	ZM1000

406664 – Assy., PCB, SYSTEMS INTERFACE, OPTION 008

REF DES	DANA P/N	DESCRIPTION			FSC	MANU P/N
	406563	ASSY	CABLE HARNESS	406563		406563
CR31	211083	DIODE	SILICO	018	21793	211083
CR32	211083	DIODE	SILICO	018	21793	211083
CR33	211083	DIODE	SILICO	018	21793	211083
CR34	211083	DIODE	SILICO	018	21793	211083
CR35	211083	DIODE	SILICO	018	21793	211083
CR36	211083	DIODE	SILICO	018	21793	211083
CR37	211083	DIODE	SILICO	018	21793	211083
CR38	211083	DIODE	SILICO	018	21793	211083
CR39	211083	DIODE	SILICO	018	21793	211083
CR41	211083	DIODE	SILICO	018	21793	211083
CR42	211083	DIODE	SILICO	018	21793	211083
CR43	211083	DIODE	SILICO	018	21793	211083
CR44	211083	DIODE	SILICO	018	21793	211083
CR45	211083	DIODE	SILICO	018	21793	211083
CR46	211083	DIODE	SILICO	018	21793	211083
CR47	211083	DIODE	SILICO	018	21793	211083
CR48	211083	DIODE	SILICO	018	21793	211083
CR49	211083	DIODE	SILICO	018	21793	211083
CR50	211083	DIODE	SILICO	018	21793	211083
J8	715091	PCB	6 PIN	715091		715091
J110	715091	PCB	15 PIN (PART OF 715091)	715091		715091
J111	715092	PCB		715092		715092
J112	715093	PCB		715093		715093
P8	600566	CONN		251-06-30-160	71785	251-06-30-160
P110	600698	CONN	15 PIN	251-15-30-260	71785	251-15-30-260
P111	600698	CONN	15 PIN	251-15-30-260	71785	251-15-30-260
P112	600698	CONN	15 PIN	251-15-30-260	71785	251-15-30-260

406660 - 662 – Assy., PCB, REAR INPUT, OPTION 010

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
J108	001803	RES 24 OHM 5% 1/8W		
J108	600567	CONN 31-236-1050	02660	31-236-1050
J109	001803	RES 24 OHM 5% 1/8W		
J109	600567	CONN 31-236-1050	02660	31-236-1050

406659 – Assy., PCB, TCXO OSCILLATOR, OPTION 050

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R76	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
W5	600245	JUMPER L-2007-1		L-2007-1
Y1	730551	OSCILLATOR CRYSTAL 730551	21793	730551
Y1	730578	OSCILLATOR CRYSTAL	11237	

406559 – Assy., PCB, TCRO OSCILLATOR, OPTION 200

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
C6	110062	CAP ELECT 500 MFD 50 V	05571	39D507G050L4
CR9	210004	DIODE SILICO SD4	12060	SD4
CR10	210004	DIODE SILICO SD4	12060	SD4
Y101	730349	OSCILLATOR SELECTED 730349	21793	730349

406130 – Assy., PCB, 28V REGULATOR, OPTION 200

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
	715130	PC BOARD			715130		21793	715130
	600591	TEST POINT						
C1	101098	CAP	CERAM	330 PFD	500 V	10%	71471	SCD1X5F
CR1	220061	DIODE	ZENER		28 V	5% 1/2W	81349	1N5255B
CR2	211083	DIODE	SILICO		018		21793	211083
Q1	200154	TRANS			MJE370		04713	MJE370
Q2	200037	TRANS	SILICO	NPN	2N3646		80131	2N3646
R1	000511	RES	CARBON	510 OHM		5% 1/4W	81349	RC07GF511J
R2	000332	RES	CARBON	3.3 K		5% 1/4W	81349	RC07GF332J

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